

# EENG 426/CPSC 459/ENAS 876 Silicon Compilation

## Non-deterministic selections

Computer Systems Lab  
<http://csl.yale.edu/~rajit>

Fall 2018

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

1 / 16

## Arbitration

Consider the following CHP program:

```
* [[  $\bar{X} \rightarrow X?x$ 
  |  $\bar{Y} \rightarrow Y?x$ 
  ];
  Z!x
]
```

When  $\bar{X}$  and  $\bar{Y}$  are both **true**, we have to pick one of them and execute the appropriate branch of the selection statement.

**Arbitration** is the mechanism that picks one of two alternatives, deciding which alternative came "first."

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

2 / 16

## Arbiters

An **arbiter** is the following process:

```
Arb( $a, b, u, v$ )  $\equiv$  * [[  $a \rightarrow u\uparrow; [\neg a]; u\downarrow$ 
  |  $b \rightarrow v\uparrow; [\neg b]; v\downarrow$ 
  ]]
```

The process does a handshake on  $(a, u)$  and  $(b, v)$ .  
Suppose we try and write production rules:

```
 $a \wedge \neg v \mapsto u\uparrow$   
 $\neg a \vee v \mapsto u\downarrow$ 
```

```
 $b \wedge \neg u \mapsto v\uparrow$   
 $\neg b \vee u \mapsto v\downarrow$ 
```

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

3 / 16

## Arbiters

To make the circuit directly implementable, we flip the sense of variables  $u$  and  $v$ .

```
 $a \wedge \neg v \mapsto \neg u\downarrow$   
 $\neg a \vee \neg v \mapsto \neg u\uparrow$ 
```

```
 $b \wedge \neg u \mapsto \neg v\downarrow$   
 $\neg b \vee \neg u \mapsto \neg v\uparrow$ 
```

$\Rightarrow$  cross-coupled NAND gates.

What happens if both  $a$  and  $b$  go up at the same time?

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

4 / 16

## Arbiters

The signals will separate eventually; however, we don't know how long it will take. It is impossible to have a circuit that decides which input switched first in bounded time.

$$\Pr[\text{time} \geq t] = Ae^{-t/\tau_0}$$

Note: the **average time** taken for signals to separate is bounded.

Since our circuits are asynchronous, we can wait until the signals separate.

Yale

AVLSI

Manohar

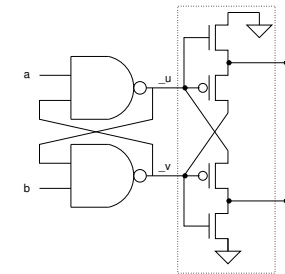
EENG 426: Silicon Compilation

Fall 2018

5 / 16

## Arbiters

The output of the cross-coupled NAND gate is connected to a filter circuit that waits for the signals to be separated by a threshold voltage.



(Note that the CMOS circuit is indeed weakly fair!)

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

6 / 16

## Arbitration

Simple example:

```
* [[  $\bar{A} \rightarrow X; A$   
  |  $\bar{B} \rightarrow Y; B$   
  ]]
```

Handshaking:

```
* [[  $ai \rightarrow xo\uparrow; [xi]; ao\uparrow; [\neg ai]; xo\downarrow; [\neg xi]; ao\downarrow$   
  |  $bi \rightarrow yo\uparrow; [yi]; bo\uparrow; [\neg bi]; yo\downarrow; [\neg yi]; bo\downarrow$   
  ]]
```

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

7 / 16

## Arbitration

Introduce new variables  $u$  and  $v$ :

```
* [[  $ai \rightarrow u\uparrow; [u]; xo\uparrow; [xi]; ao\uparrow;$   
  |  $[\neg ai]; u\downarrow; [\neg u]; xo\downarrow; [\neg xi]; ao\downarrow$   
  
  |  $bi \rightarrow v\uparrow; [v]; yo\uparrow; [yi]; bo\uparrow;$   
  |  $[\neg bi]; v\downarrow; [\neg v]; yo\downarrow; [\neg yi]; bo\downarrow$   
  ]]
```

The idea is to introduce the output of the arbiter into the handshaking expansion. The next step is to decompose the arbiter out of the handshaking expansion.

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

8 / 16

## Process factorization

Idea: “factor out” an arbiter!

After process factorization:

$$* [[ ai \rightarrow u\uparrow; [\neg ai]; u\downarrow \\ | bi \rightarrow v\uparrow; [\neg bi]; v\downarrow \\ ]]$$

||

$$* [[ u \rightarrow xo\uparrow; [xi]; ao\uparrow; [\neg u]; xo\downarrow; [\neg xi]; ao\downarrow \\ | v \rightarrow yo\uparrow; [yi]; bo\uparrow; [\neg v]; yo\downarrow; [\neg yi]; bo\downarrow \\ ]]$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

9 / 16

## Process factorization

Production rules:

$$\neg bo \wedge u \mapsto xo\uparrow \\ xi \mapsto ao\uparrow \\ (bo \vee) \neg u \mapsto xo\downarrow \\ \neg xi \mapsto ao\downarrow$$
$$\neg ao \wedge v \mapsto yo\uparrow \\ yi \mapsto bo\uparrow \\ (ao \vee) \neg v \mapsto yo\downarrow \\ \neg yi \mapsto bo\downarrow$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

10 / 16

## Arbitration with multiplexing

CHP Program:

$$* [[ \bar{A} \rightarrow S; A \\ | \bar{B} \rightarrow S; B \\ ]]$$

Decomposition:

$$* [[ \bar{A} \rightarrow P; A \\ | \bar{B} \rightarrow Q; B \\ ]]$$

||

$$* [[ \bar{P} \rightarrow S; P \\ | \bar{Q} \rightarrow S; Q \\ ]]$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

11 / 16

## Arbitration with multiplexing

Handshaking:

$$* [[ pi \rightarrow so\uparrow; [si]; po\uparrow; [\neg pi]; so\downarrow; [\neg si]; po\downarrow \\ | qi \rightarrow so\uparrow; [si]; qo\uparrow; [\neg qi]; so\downarrow; [\neg si]; qo\downarrow \\ ]]$$

Production rules:

$$pi \vee qi \mapsto so\uparrow \qquad si \wedge qi \mapsto qo\uparrow \\ \neg pi \wedge \neg qi \mapsto so\downarrow \qquad (\neg qi \wedge) \neg si \mapsto qo\downarrow$$
$$si \wedge pi \mapsto po\uparrow \\ (\neg pi \wedge) \neg si \mapsto po\downarrow$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

12 / 16

## Negated probes

Consider the following CHP program:

$$*[[\bar{X} \wedge \bar{S} \rightarrow S!true, X \\ | \neg \bar{X} \wedge \bar{S} \rightarrow S!false \\ ]]$$

This program determines the current value of the probe.  
S determines when the probe is evaluated.

- Why a thin bar?!

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

13 / 16

## Negated probes

Assuming the channels are passive, we get the following handshaking expansion:

$$*[[Xi \wedge Si \rightarrow Sto\uparrow; [\neg Si]; Sto\downarrow; Xo\uparrow; [\neg Xi]; Xo\downarrow \\ | \neg Xi \wedge Si \rightarrow Sfo\uparrow; [\neg Si]; Sfo\downarrow \\ ]]$$

Since the CMOS implementation of a two-way arbiter is weakly fair, we can implement this HSE with the following:

$$*[[Xi \rightarrow [Si]; Sto\uparrow; [\neg Si]; Sto\downarrow; Xo\uparrow; [\neg Xi]; Xo\downarrow \\ | Si \rightarrow Sfo\uparrow; [\neg Si]; Sfo\downarrow \\ ]]$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

14 / 16

## Negated probes

Introduce arbiter variables:

$$*[[Xi \rightarrow u\uparrow; [u]; [Si]; Sto\uparrow; [\neg Si]; Sto\downarrow; \\ Xo\uparrow; [\neg Xi]; u\downarrow; [\neg u]; Xo\downarrow \\ | Si \rightarrow v\uparrow; [v]; Sfo\uparrow; [\neg Si]; v\downarrow; [\neg v]; Sfo\downarrow \\ ]]$$

Apply process factorization:

$$*[[u \rightarrow [Si]; Sto\uparrow; [\neg Si]; Sto\downarrow; Xo\uparrow; [\neg u]; Xo\downarrow \\ | v \rightarrow Sfo\uparrow; [\neg v]; Sfo\downarrow \\ ]]$$

||

$$Arb(Xi, Si, u, v)$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

15 / 16

## Negated probes

Reshuffled HSE:

$$*[[u \rightarrow [Ei]; Eto\uparrow; [\neg Ei]; Xo\uparrow; Eto\downarrow; [\neg u]; Xo\downarrow \\ | v \rightarrow Efo\uparrow; [\neg v]; Efo\downarrow \\ ]]$$

Production rules:

$$u \wedge \neg Xo \wedge Ei \mapsto \neg Eto\downarrow \qquad Xo \mapsto \neg Xo\downarrow \\ \neg Xo \mapsto \neg Eto\uparrow \qquad \neg Xo \mapsto \neg Xo\uparrow$$

$$\neg Xo \wedge v \mapsto Efo\downarrow \qquad u \mapsto \neg u\downarrow \\ \neg v \mapsto Efo\uparrow \qquad \neg u \mapsto \neg u\uparrow$$

$$\neg \neg u \wedge \neg \neg Eto \wedge \neg Ei \mapsto Xo\uparrow \\ \neg u \wedge \neg Eto \mapsto Xo\downarrow$$

Yale

AVLSI

Manohar

EENG 426: Silicon Compilation

Fall 2018

16 / 16