Introduction to Asynchronous Design

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Approaches to computation

	Discrete Time	Continuous Time
Discrete Value	Digital, synchronous logic	**Digital, asynchronous logic**
Continuous Value	Switched-capacitor analog	General analog computation

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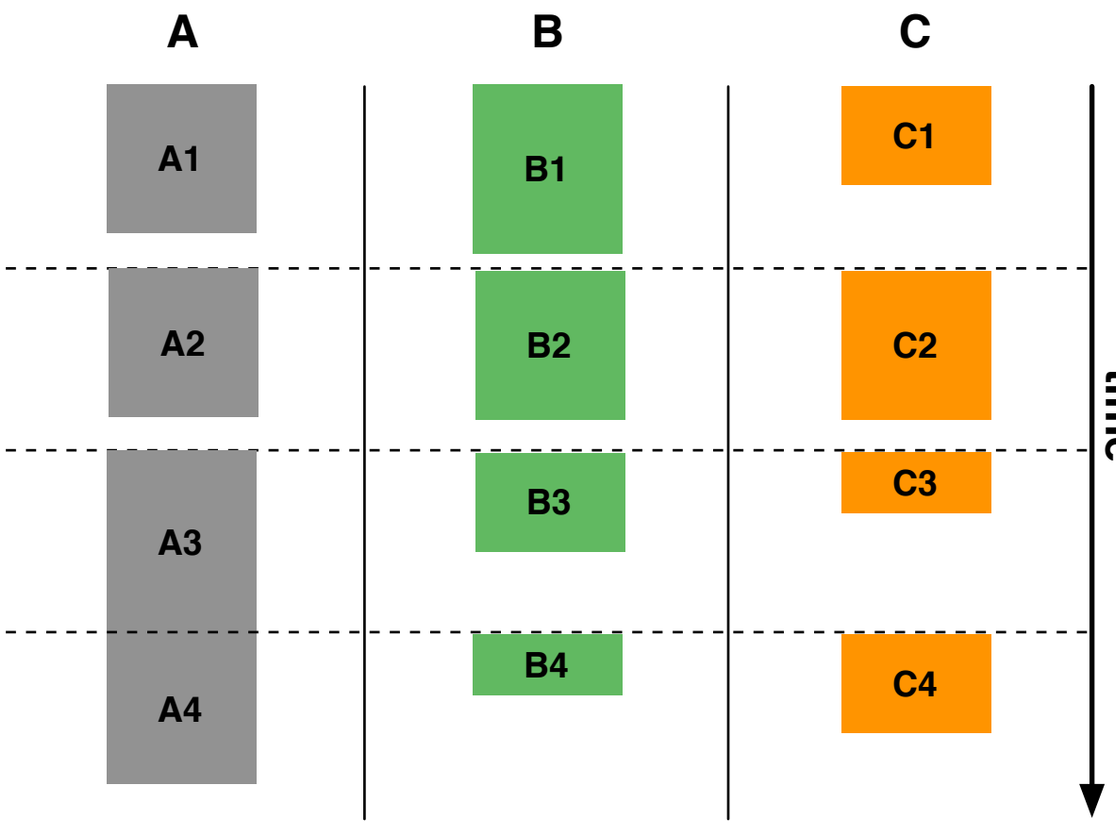
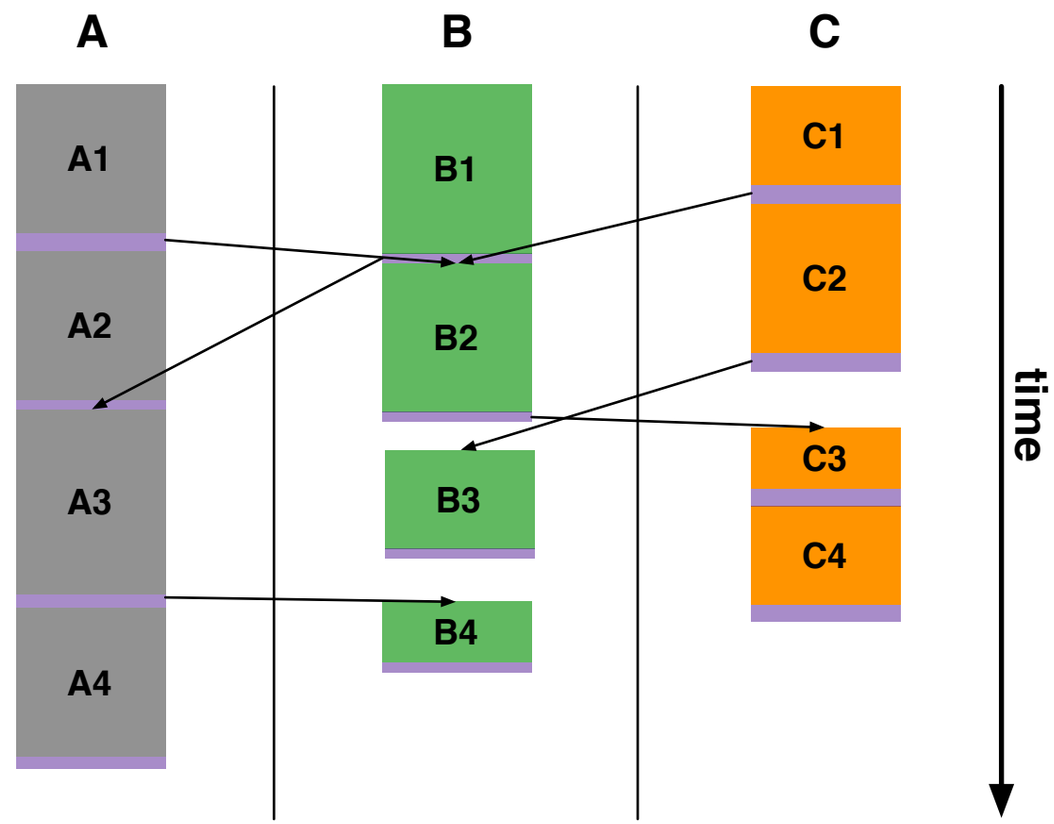
Explicit versus implicit synchronization



Synchronous computation



Asynchronous computation

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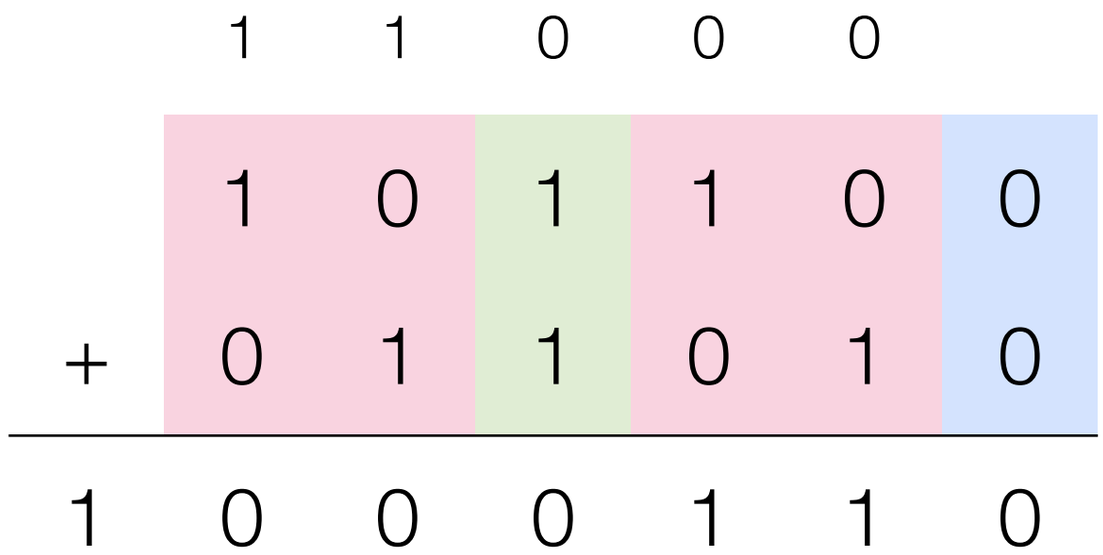
I. The gap between average and max delay

- Slow part: computing carries
  - … but only in the worst-case!



Theorem [von Neumann, 1946]. The average-case latency for a ripple carry binary adder is O(log N) for i.i.d. inputs

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A.W. Burks, H.H. Goldstein, J. von Neumann. Preliminary discussion of the logical design of an electronic computing instrument. (1946)

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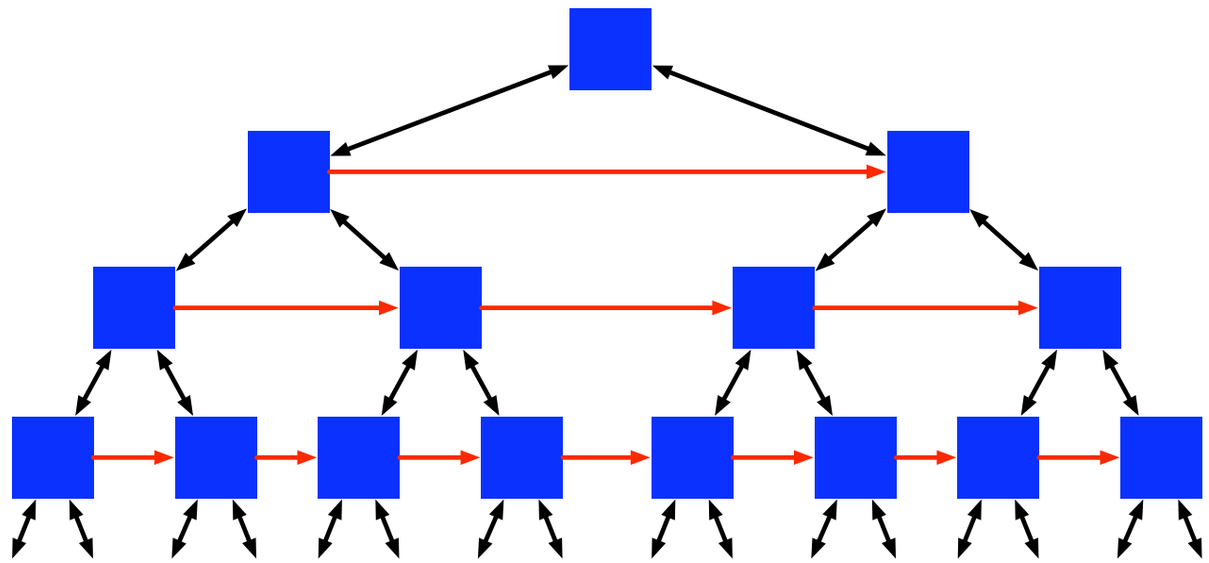
I. The gap between average and max delay

- Standard adder tree
  - ❖ O(log N) latency
- Hybrid adder tree
  - ❖ Tree adder + ripple adder



Theorem [Winograd, 1965]. The worst-case latency for binary addition is Ω(log N)

Theorem. The average-case latency of the hybrid asynchronous adder is O(log log N) for i.i.d. inputs

Theorem. The average-case latency of the hybrid asynchronous adder is optimal for *any* input distribution

S.O. Winograd. On the time required to perform addition. JACM (1965)

R. Manohar and J. Tierno. Asynchronous parallel prefix computation. IEEE Transactions on Computers (1998)

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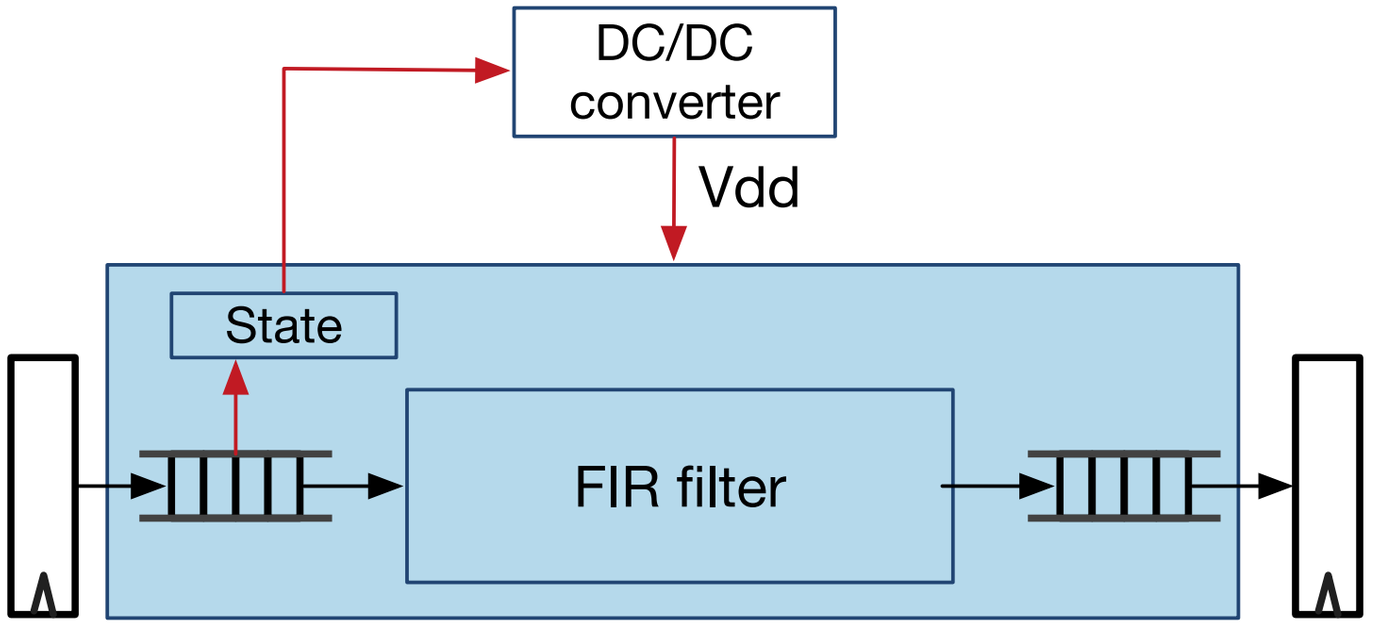
II. Data-driven power management

- Low power FIR filter
  - ❖ External, synchronous I/O
  - ❖ Monitor occupancy of FIFOs
  - ❖ Speed up/slow down using adaptive power supply
- Break-point add/multiply
  - ❖ Detect when top half of operand is required
  - ❖ Dynamically switch between full width and half width arithmetic

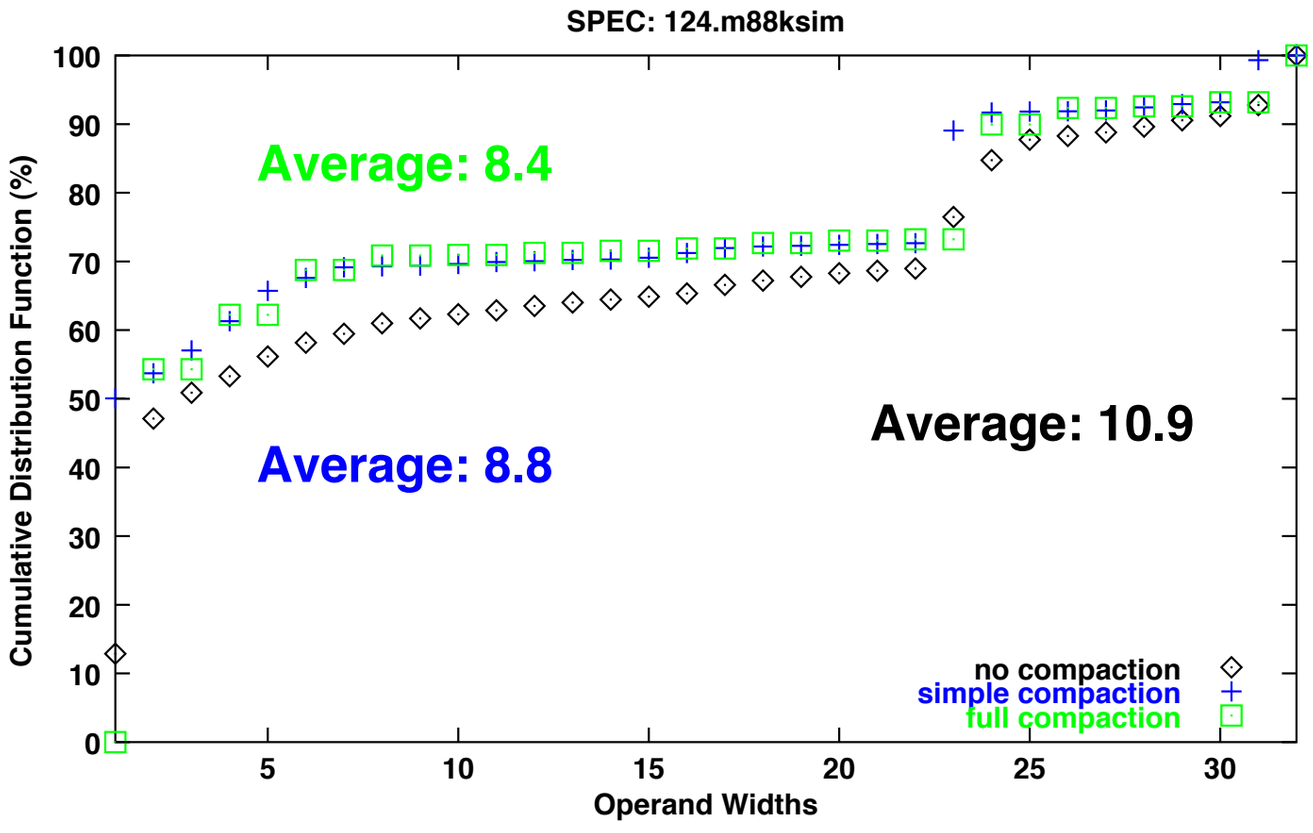


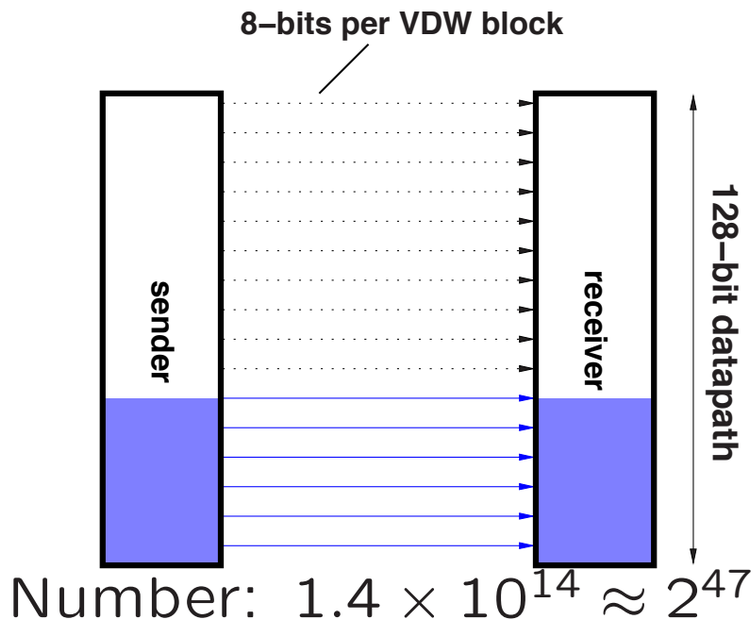
L. Nielsen and J. Sparso. A Low-power Asynchronous Datapath for a FIR filter bank. Proc. ASYNC (1996)

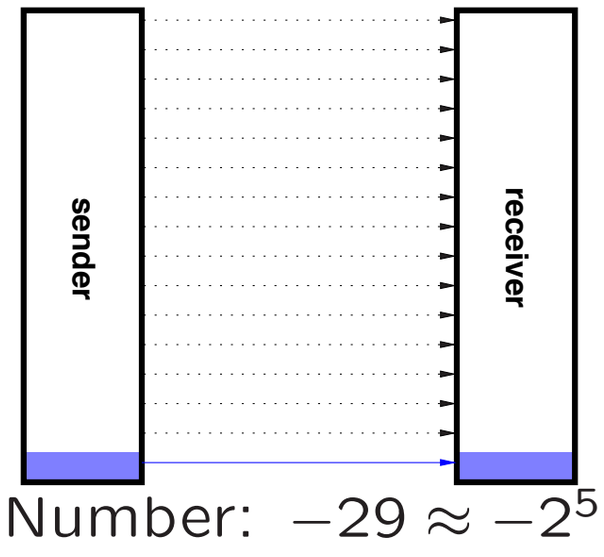
II. Data-driven power management

- Width-adaptive numbers
  - ❖ Compress leading 0's and 1's

$$\begin{array}{rcccccccc} & 0 & 0 & 0 & \cdots & 0 & 0 & 0 & 1 \\ + & 0 & 0 & 0 & \cdots & 0 & 0 & 0 & 1 \\ \hline & 0 & 0 & 0 & \cdots & 0 & 0 & 1 & 0 \end{array} \quad \text{v/s} \quad \begin{array}{rccc} & & \underline{0} & 1 \\ + & & \underline{0} & 1 \\ \hline & \underline{0} & 1 & 0 \end{array}$$







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R. Manohar. Width-Adaptive Data Word Architectures. Proc. ARVLSI (2001)

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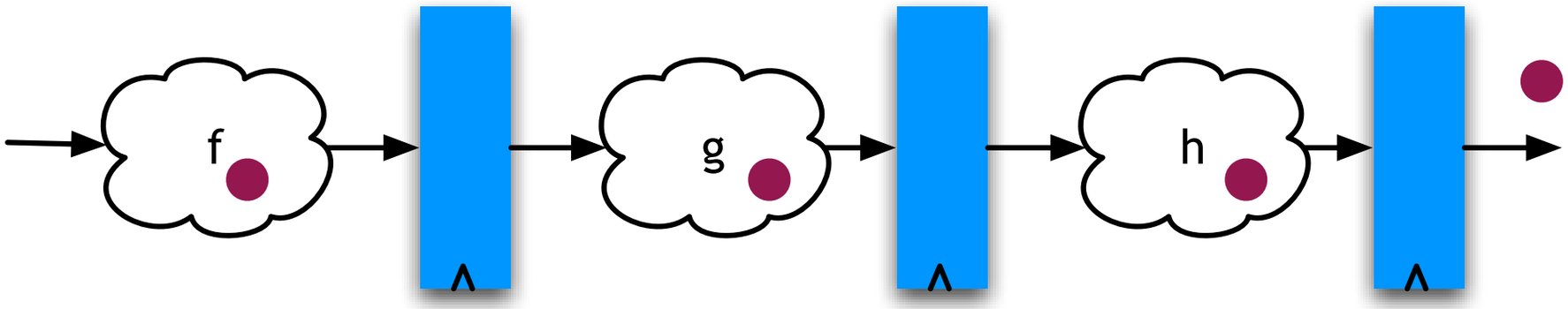
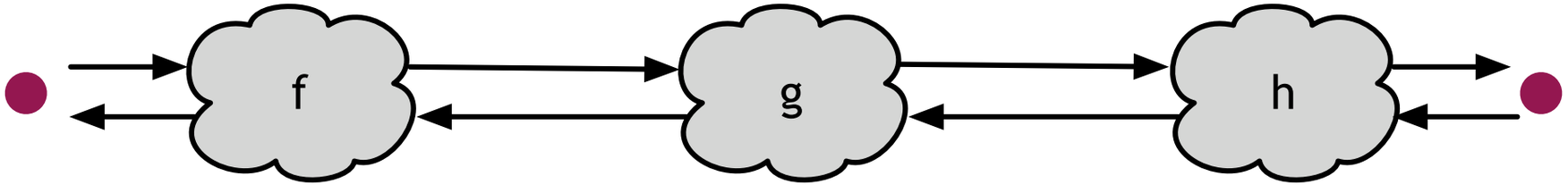
III. Elasticity of pipelines



Asynchronous computation is robust to changes in circuit-level pipelining!*



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*R. Manohar, A. J. Martin. Slack Elasticity in Concurrent Computing. Proc. Mathematics of Program Construction (1998)

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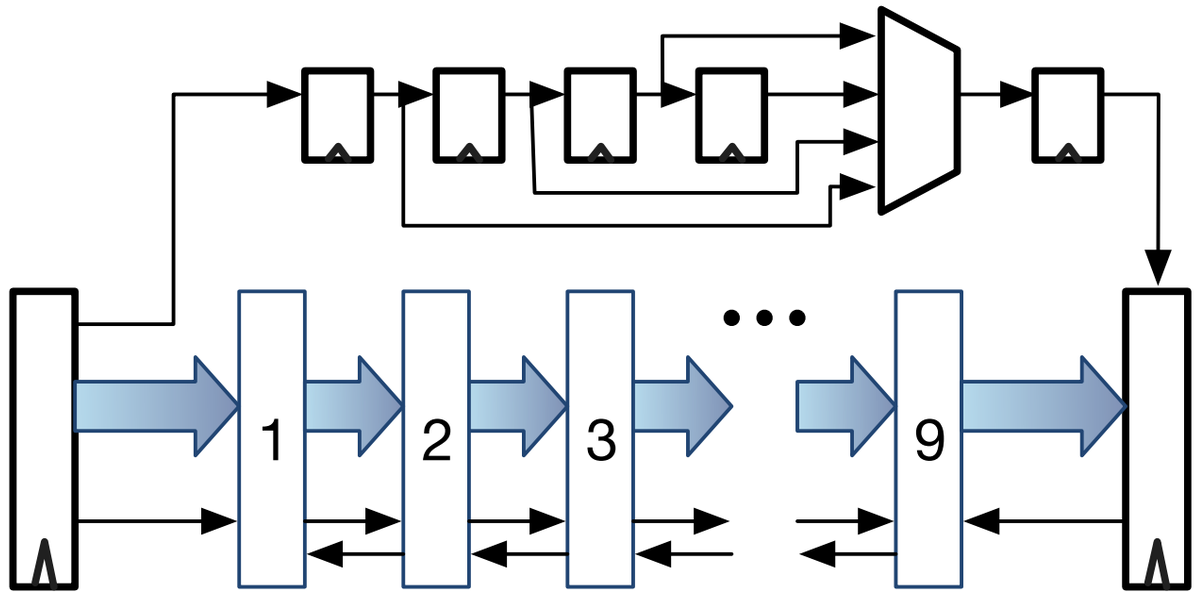
III. Elasticity of pipelines

- Asynchronous FIR filter
  - Data arrives at variable rates
  - Data rates are *predictable*
- Fixed amount of *time* for async computation
- Variable number of *clock cycles* for the fixed time budget



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M. Singh, J.A. Tierno, A. Rylyakov, S. Rylov, S.M. Nowick. An adaptively pipelined mixed synchronous-asynchronous digital FIR filter chip operating at 1.3 GHz. Proc. ASYNC (2002)

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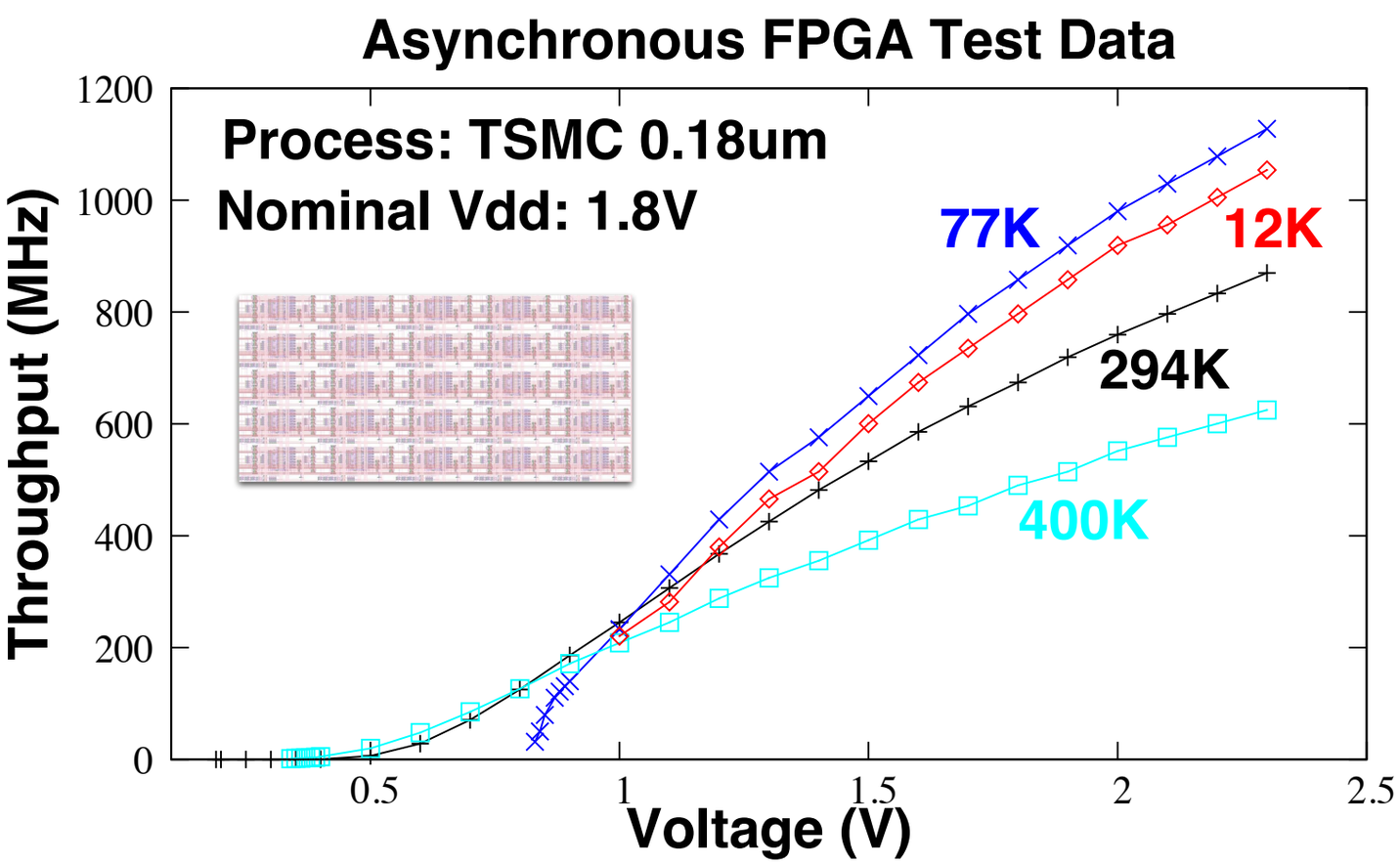
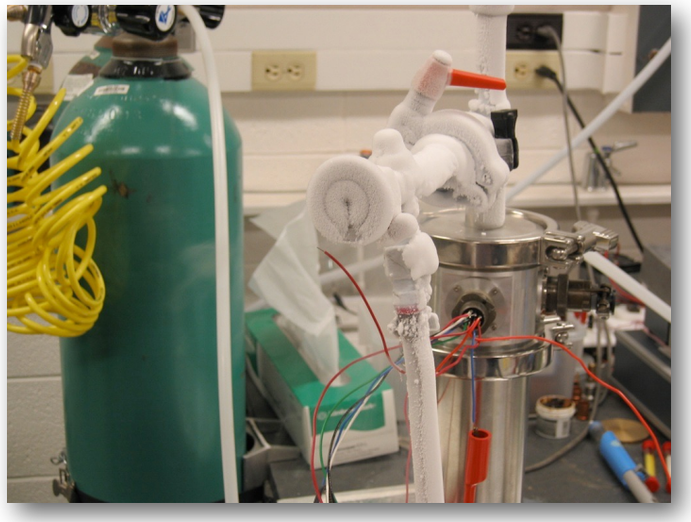
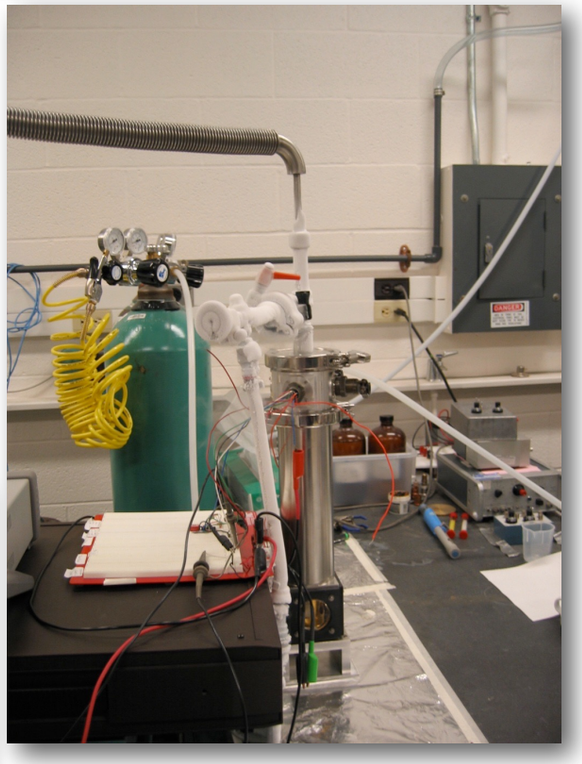
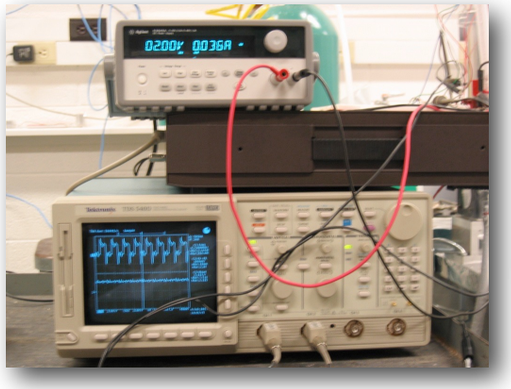
IV. Timing robustness



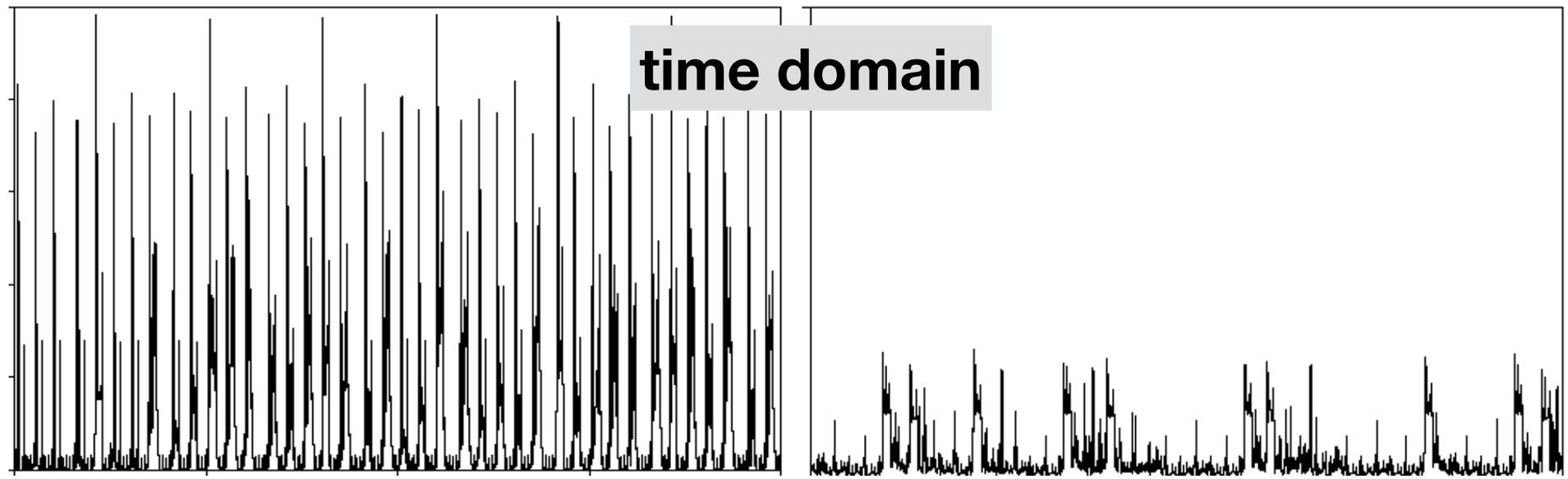






D. Fang, J. Teifel, and R. Manohar. A High-Performance Asynchronous FPGA: Test Results. Proc. FCCM (2005)

V. Low noise and low EMI



Synchronous 80C51 (Philips)

Asynchronous 80C51 (Philips)

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J. Kessels, T. Kramer, G. den Besten, A. Peeters, V. Timm. Applying Asynchronous Circuits in Contactless Smart Cards. Proc. ASYNC (2000)

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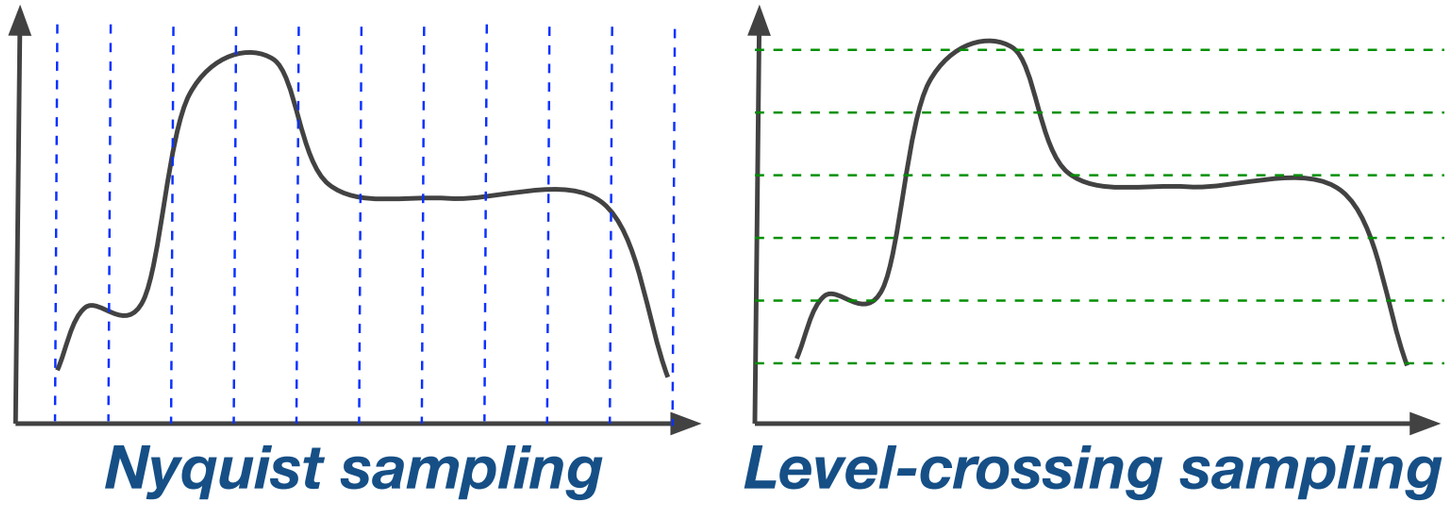
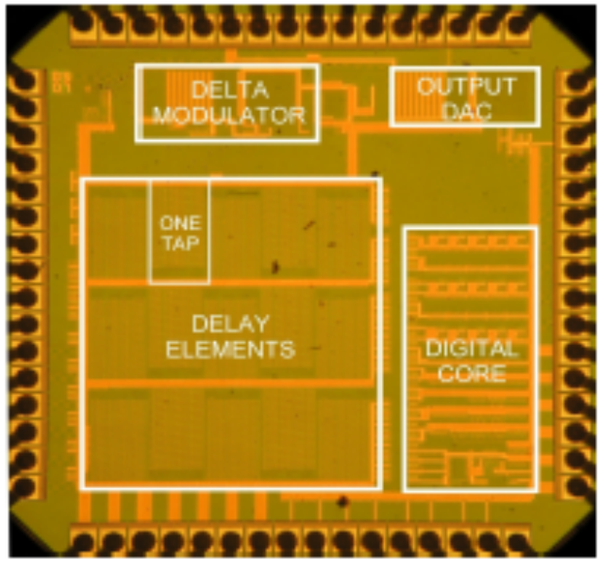
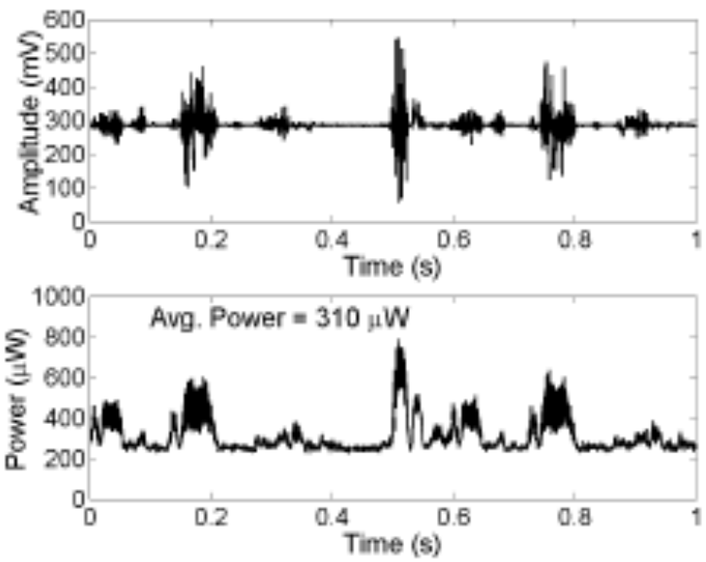
VI. Continuous-time information processing

- Continuous-time digital signal processing
- Automatic adaptation to input bandwidth
- No aliasing from sampling process







B. Schell, Y. Tsividis. A clockless adc/dsp/dac system with activity-dependent power dissipation and no aliasing. Proc. ISSCC (2008)

Y. Chen, X. Zhang, Y. Lian, R. Manohar, Y. Tsividis. A Continuous-Time Digital IIR Filter with Signal-Derived Timing and Fully Agile Power Consumption. *IEEE Journal of Solid-State Circuits,* 53(2):418-430 *(JSSC)*, February 2018.

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