Links and Joints

PART 2: gate-level design

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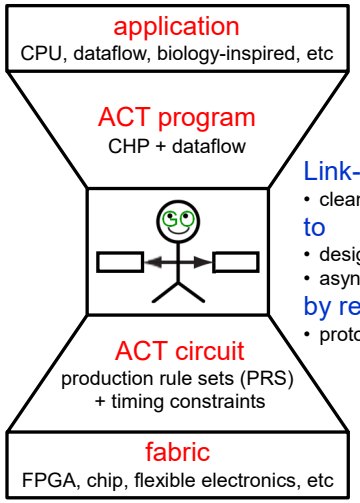
1

Reminder: context



Link-Joint network
- clean interface

to
- design and test
- asynchronous circuits

by refining
- protocols, families, etc.

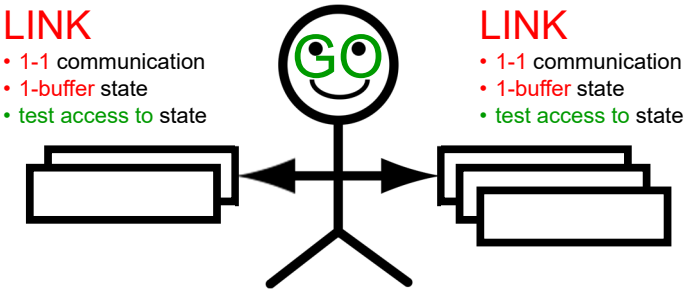
After: Kees van Berkel, Handshake Circuits, Fig. 1.1. Cambridge University Press, 1993.

4

Reminder: Links and Joints

LINK
- 1-1 communication
- 1-buffer state
- test access to state

LINK
- 1-1 communication
- 1-buffer state
- test access to state



- Joint-specific (no)GO
- computation
- flow control

JOINT

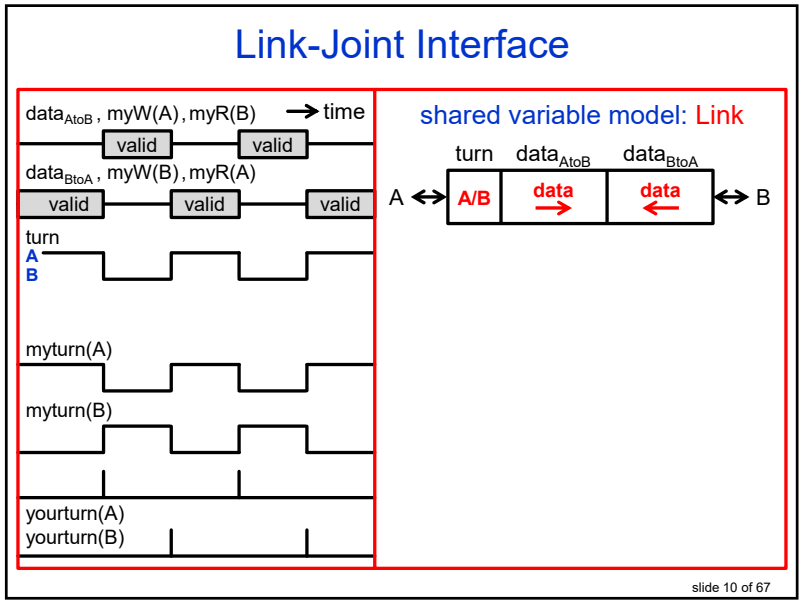
"a place where Links meet to exchange information"

6

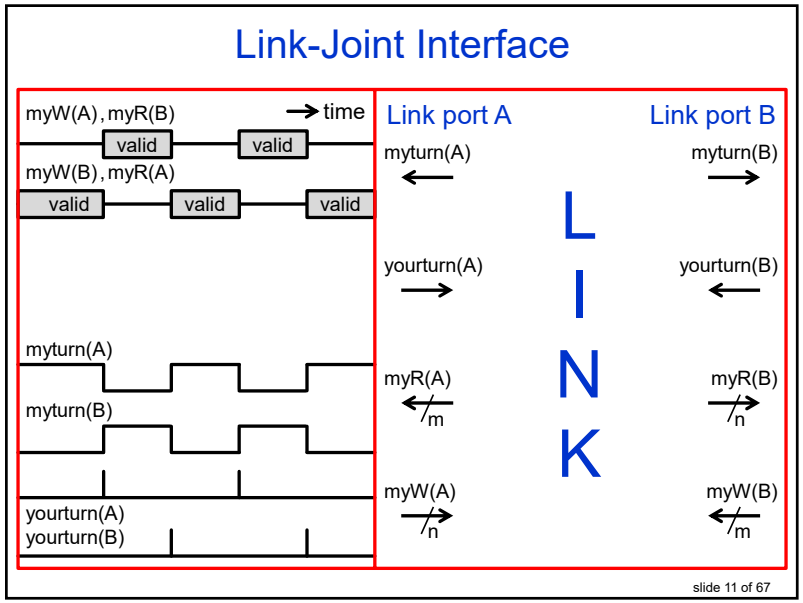
Link-Joint interface

- abstract shared variable model
- gate-level communication model
- ~~relative timing constraints~~

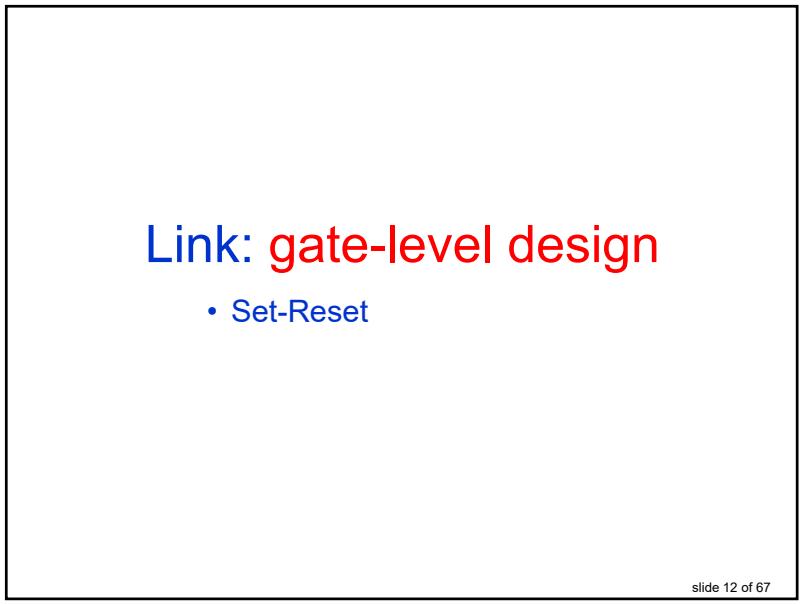
7


Link-Joint Interface
data$_{AtoB}$, myW(A) , myR(B)
time
valid
valid
data$_{BtoA}$, myW(B) , myR(A)
valid
valid
valid
turn
A
B
myturn(A)
myturn(B)
yourturn(A)
yourturn(B)
shared variable model: Link
turn
data$_{AtoB}$
data$_{BtoA}$
A
A/B
data
data
B
slide 10 of 67

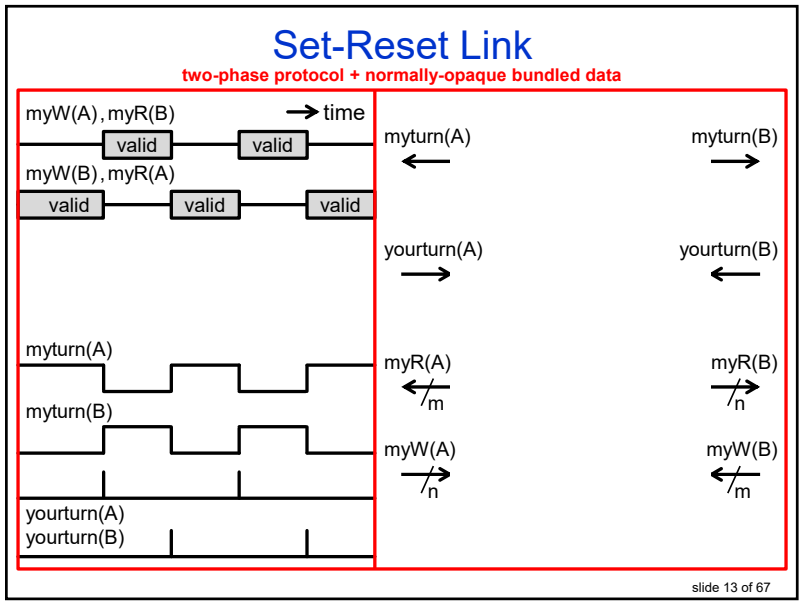
10


Link-Joint Interface
myW(A) , myR(B)
time
valid
valid
myW(B) , myR(A)
valid
valid
valid
myturn(A)
myturn(B)
yourturn(A)
yourturn(B)
Link port A
Link port B
myturn(A)
myturn(B)
yourturn(A)
yourturn(B)
myR(A)
myR(B)
myW(A)
myW(B)
m
n
n
m
L
I
N
K
slide 11 of 67

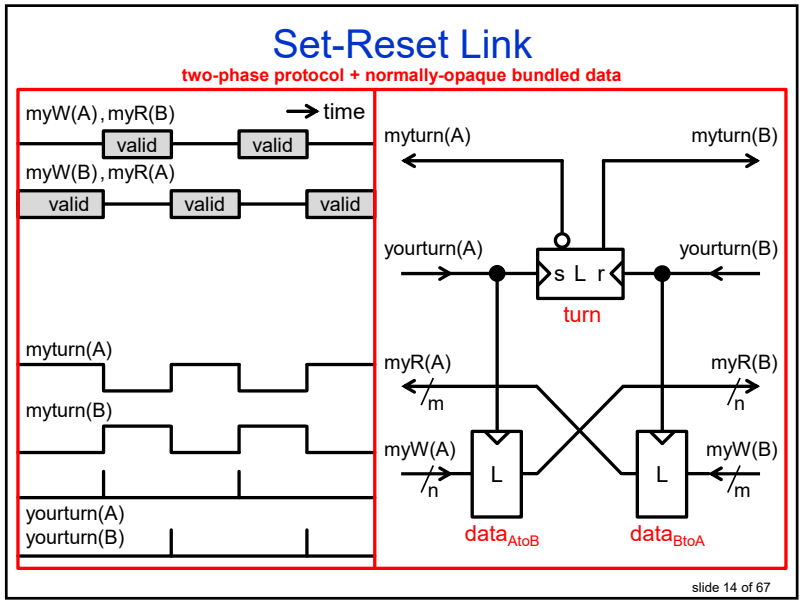
11


Link: gate-level design
• Set-Reset
slide 12 of 67

12


Set-Reset Link
two-phase protocol + normally-opaque bundled data
myW(A) , myR(B)
time
valid
valid
myW(B) , myR(A)
valid
valid
valid
myturn(A)
myturn(B)
yourturn(A)
yourturn(B)
myturn(A)
myturn(B)
yourturn(A)
yourturn(B)
myR(A)
myR(B)
myW(A)
myW(B)
m
n
n
m
slide 13 of 67

13



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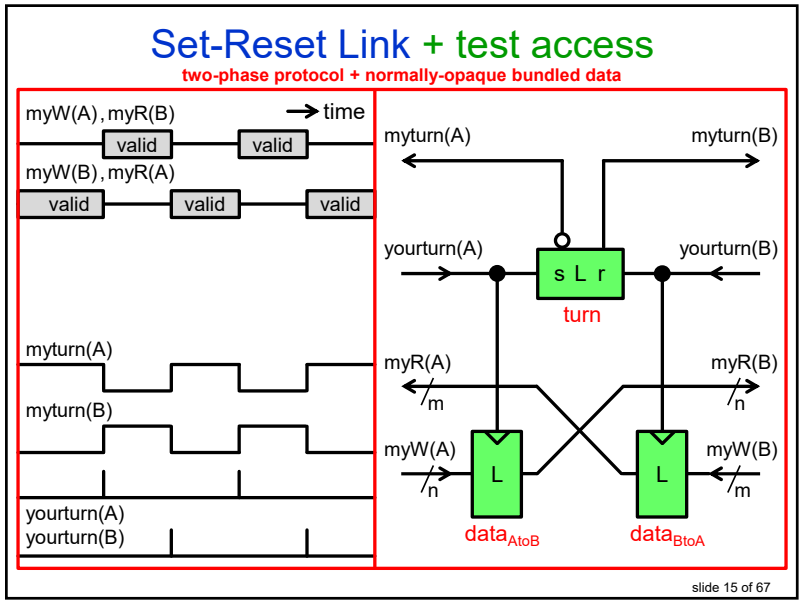


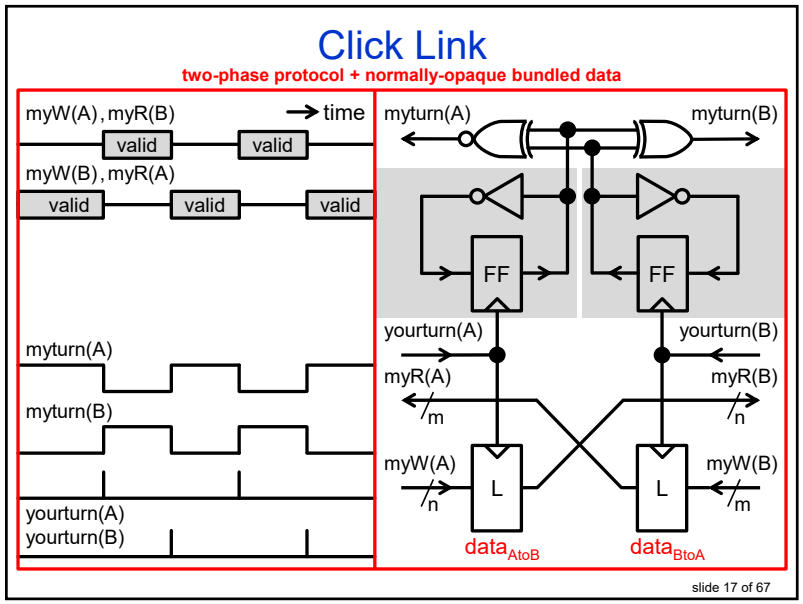
15

Link: gate-level design

- Set-Reset
- Click

slide 16 of 67

16



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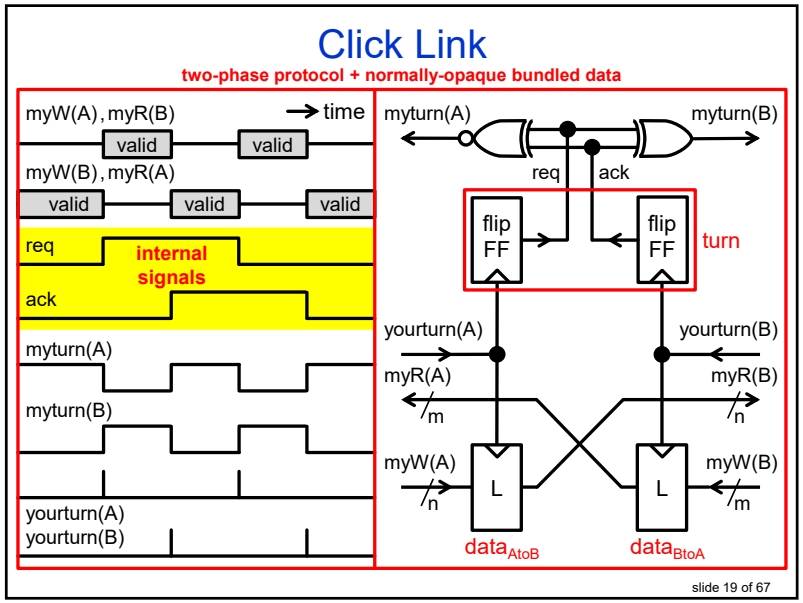

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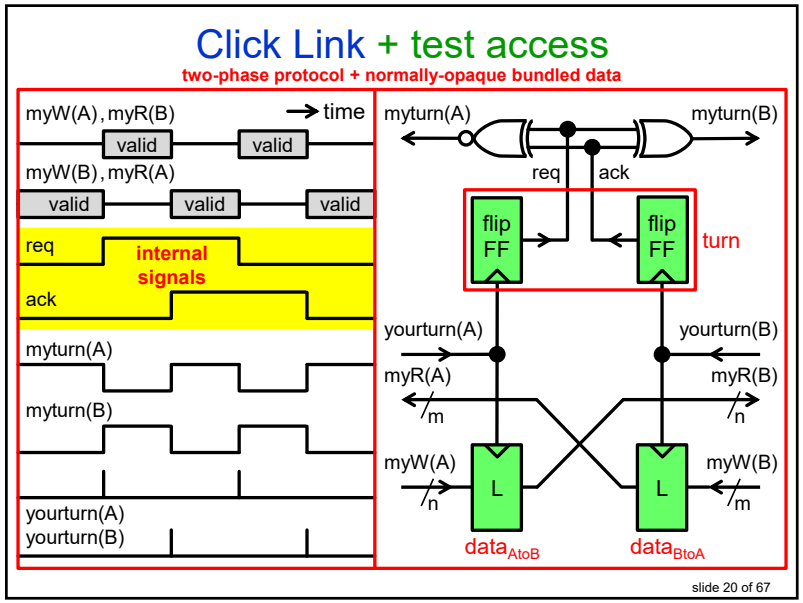


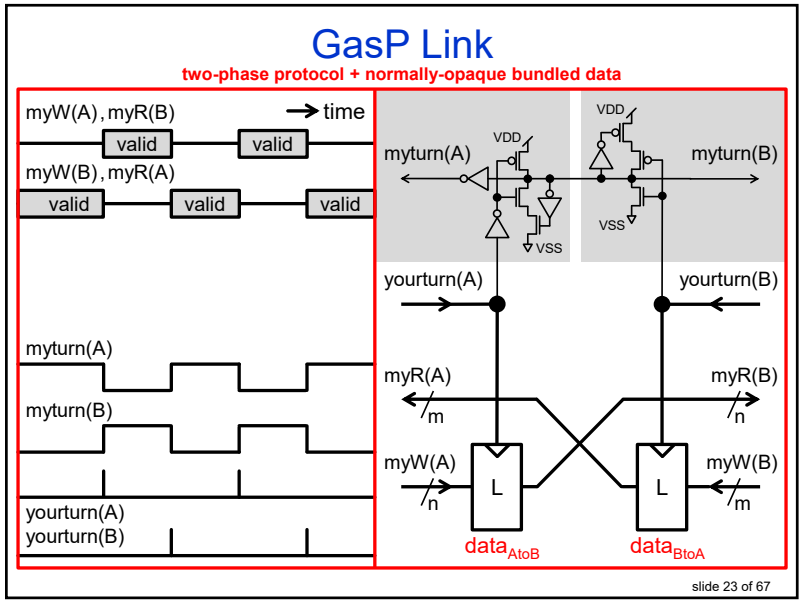
20

Link: gate-level design

- Set-Reset
- Click
- GasP

slide 22 of 67

22



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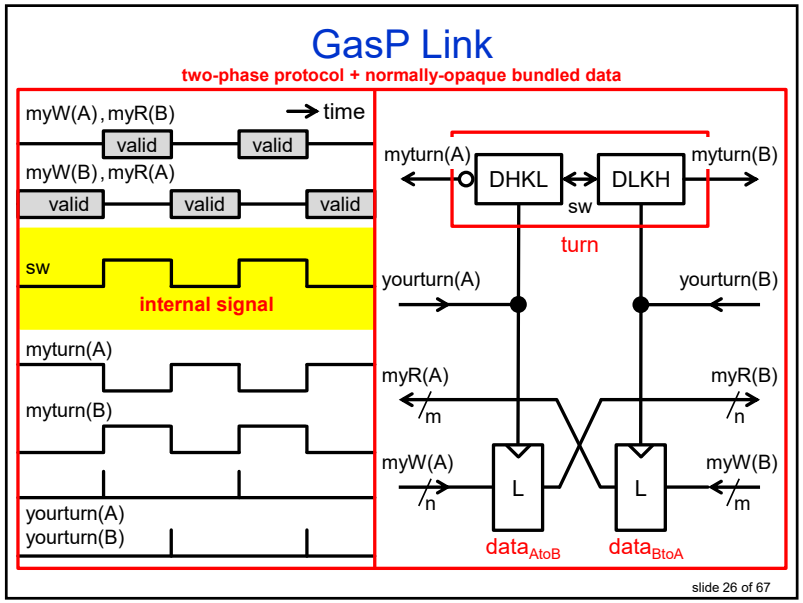

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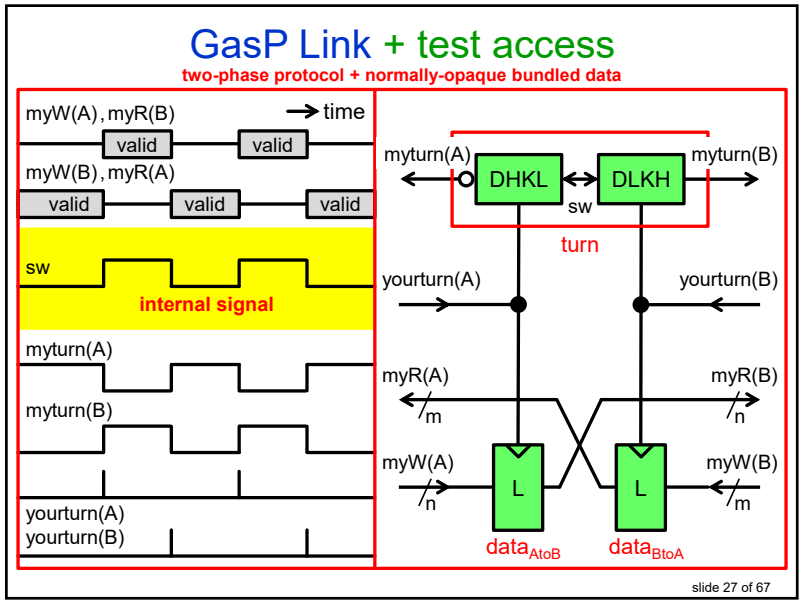


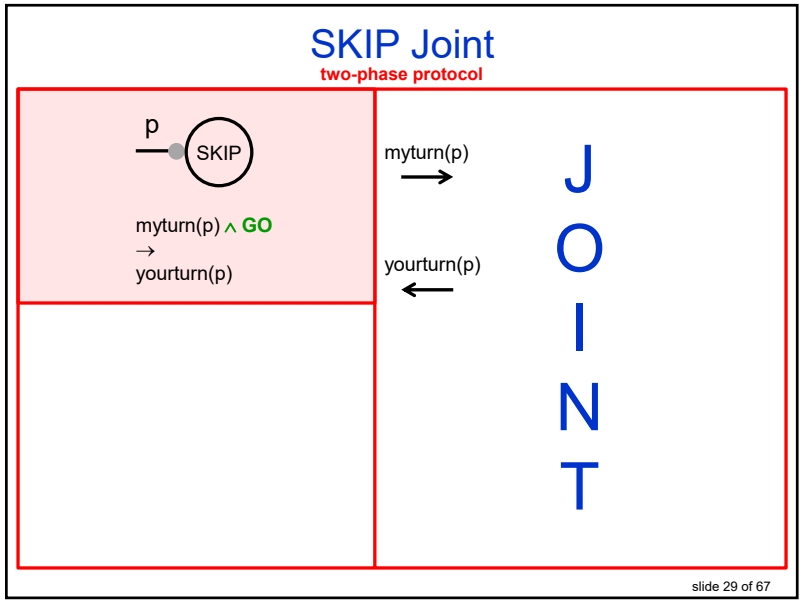
27

Joint: gate-level design

- without data

slide 28 of 67

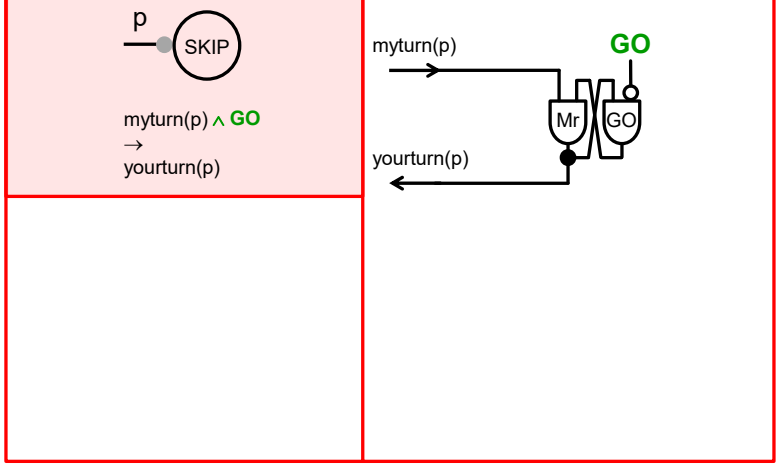
28



29

SKIP Joint + test access

two-phase protocol



slide 31 of 67

31

Joint: gate-level design

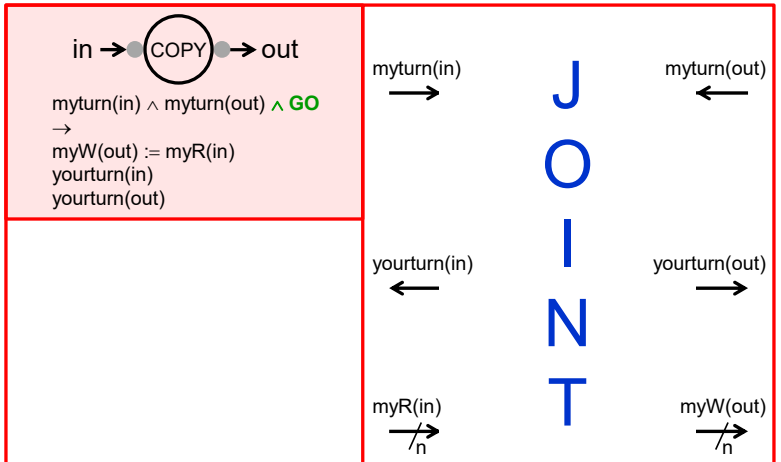
- without data
- with data

slide 32 of 67

32

COPY Joint

two-phase protocol + bundled data

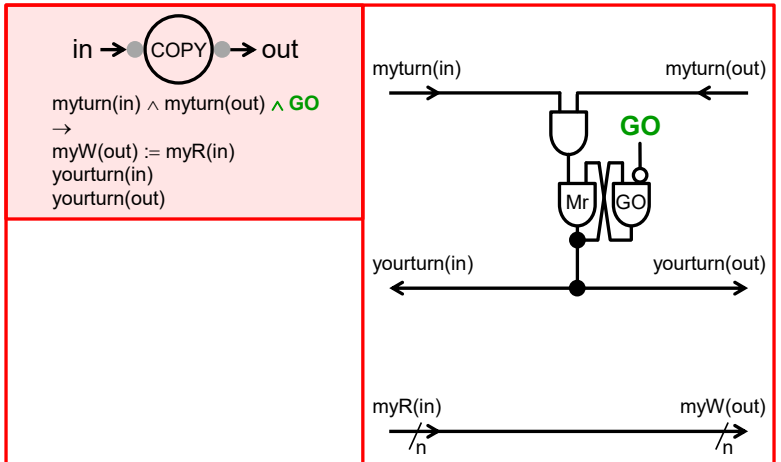


slide 34 of 67

34

COPY Joint

two-phase protocol + bundled data



slide 35 of 67

35

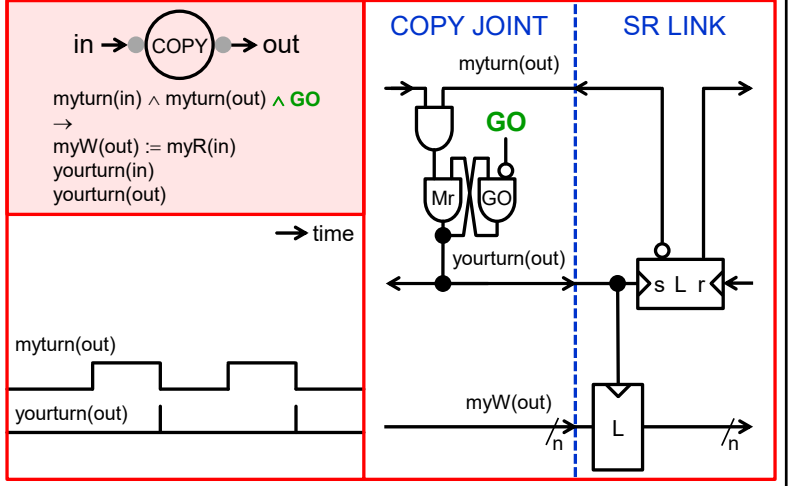
Link-Joint

gate-level communication model

slide 36 of 67

36

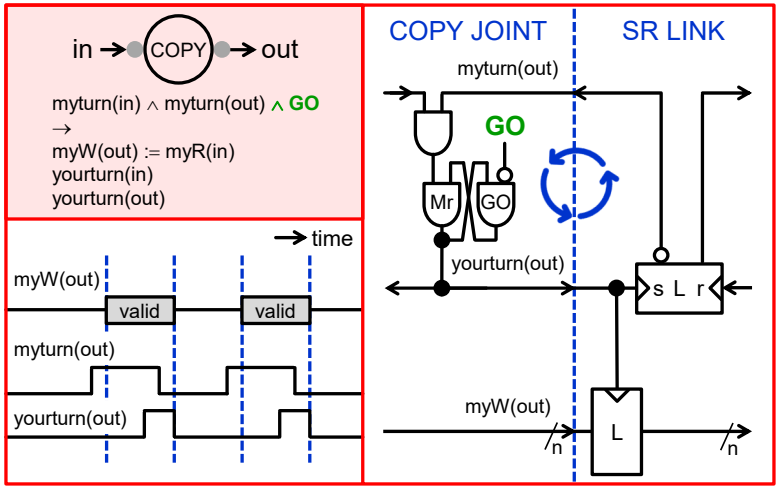
Gate-level communication model



slide 37 of 67

37

Gate-level communication model



slide 38 of 67

38

Gate-level communication model

[Chau et al., A Framework for Asynchronous Circuit Modeling and Verification in ACL2, HVC 2017]

2-step interleaving model:

step 1 ("rise")

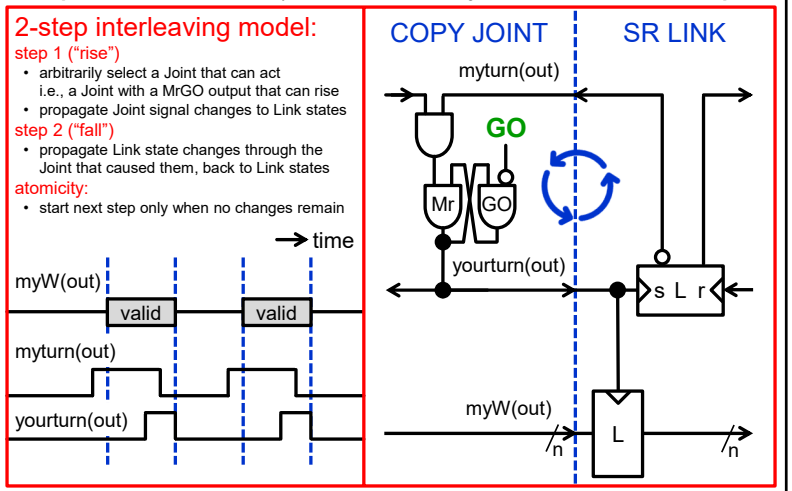
- arbitrarily select a Joint that can act
  i.e., a Joint with a MrGO output that can rise
- propagate Joint signal changes to Link states

step 2 ("fall")

- propagate Link state changes through the Joint that caused them, back to Link states

atomicity:

- start next step only when no changes remain



slide 39 of 67

39

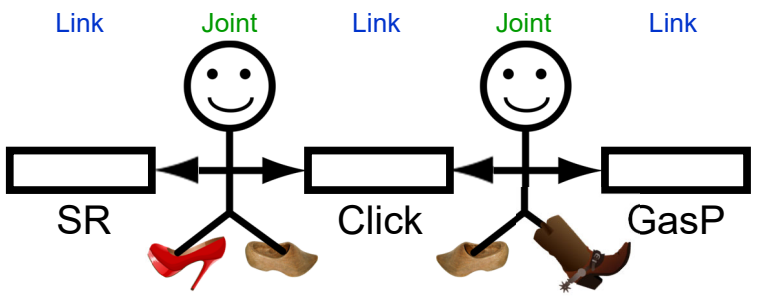
Time for 1-2 questions

40

Mixing circuit families

41

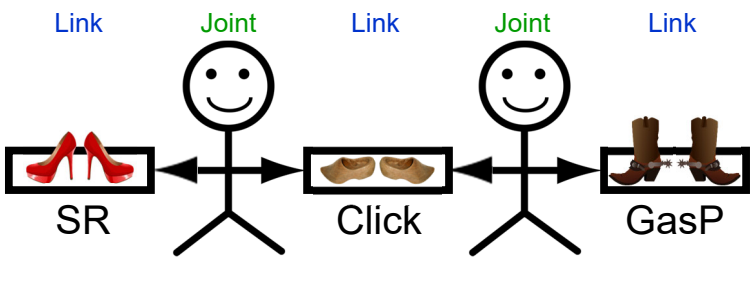
Mixing circuit families



WRONG Link-Joint picture
- Differences in circuit families are internal to Links
- The Link-Joint interface is always the same

46

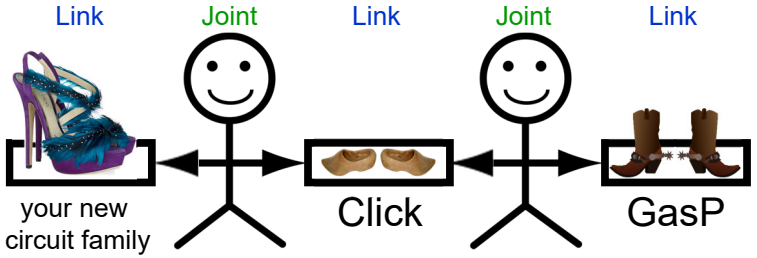
Mixing circuit families



RIGHT Link-Joint picture
- Differences in circuit families are internal to Links
- The Link-Joint interface is always the same

47

Mixing circuit families



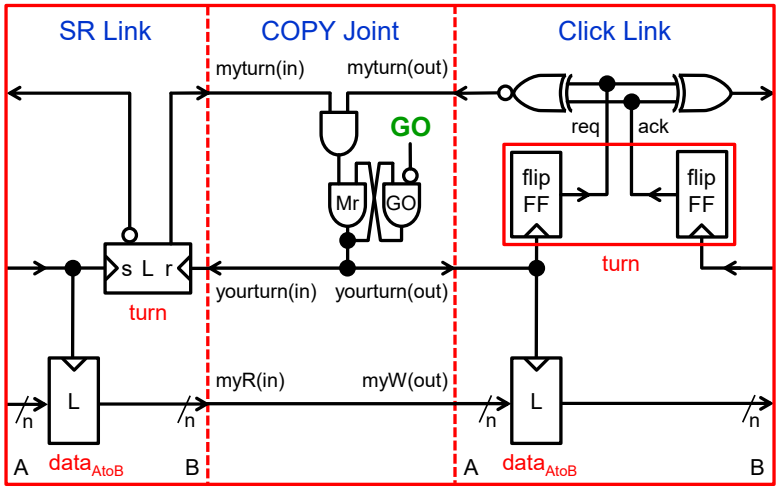
RIGHT Link-Joint picture

- Differences in circuit families are internal to Links
- The Link-Joint interface is always the same

slide 48 of 67

48

Mixing circuit families: example



slide 49 of 67

49

Time for 1-2 questions

slide 50 of 67

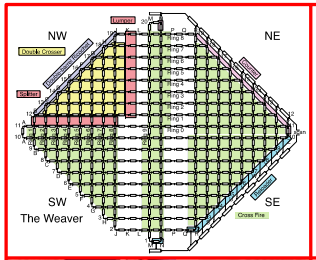
50

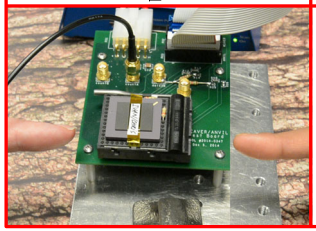
External test access

slide 51 of 67

51

External test access





To test software
- so many lines – so few exports

use
- interactive code debug
- to set states
- and breakpoints for single-step code, etc.

combine the best of both worlds

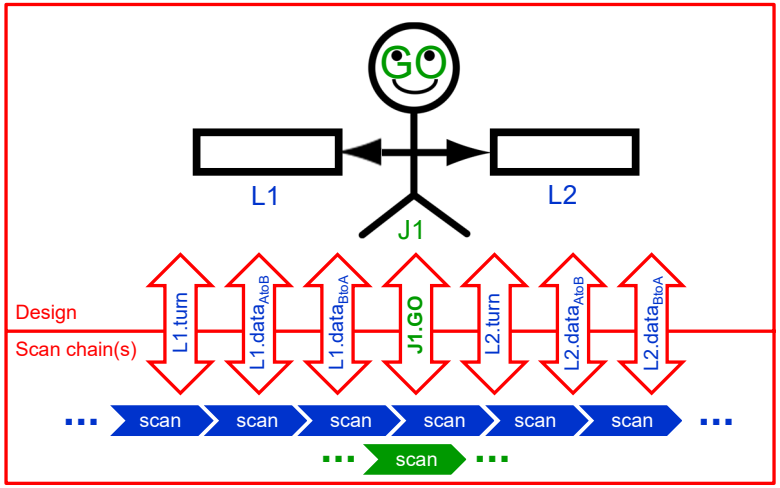
To test hardware
- so many wires – so few pins

use
- scan to share pins to read and write states/GO
- MrGO to control actions

slide 54 of 67

54

External test access: scan



slide 56 of 67

56

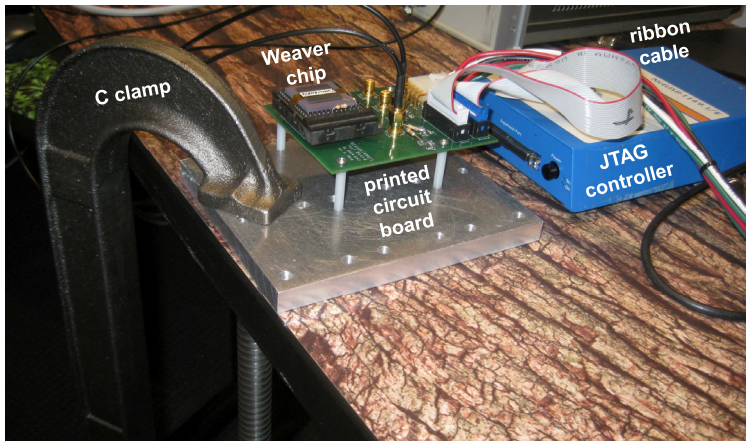
Measurements of throughput and power

[Roncken-Sutherland, Design and test of high-speed asynchronous circuits, J. Di and S.C. Smith (Eds.): Asynchronous Circuit Applications, Chapter 7, The Institute of Engineering and Technology (IET), 2020]

slide 57 of 67

57

The Weaver test chip (2015)

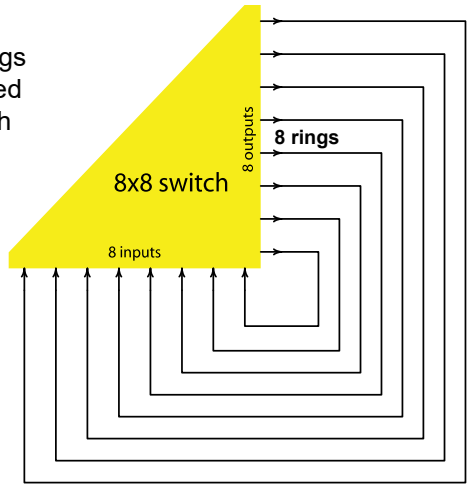


slide 58 of 67

58

Weaver overview

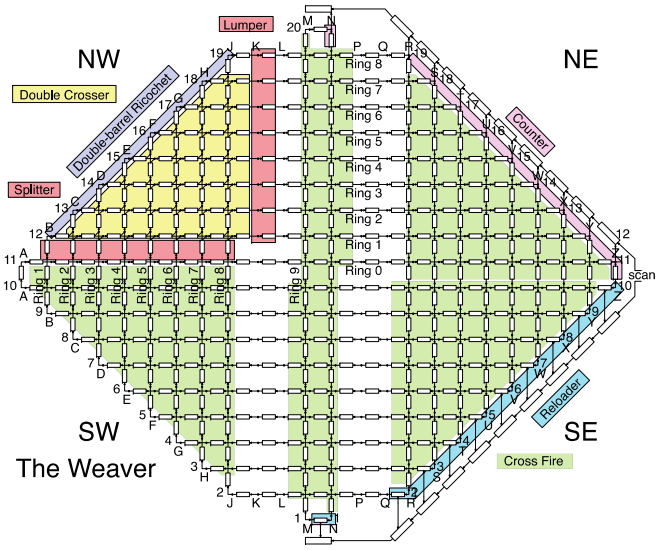
8 recirculating rings provide high-speed data for the switch



Not shown:
2 more rings
without switches

slide 59 of 67

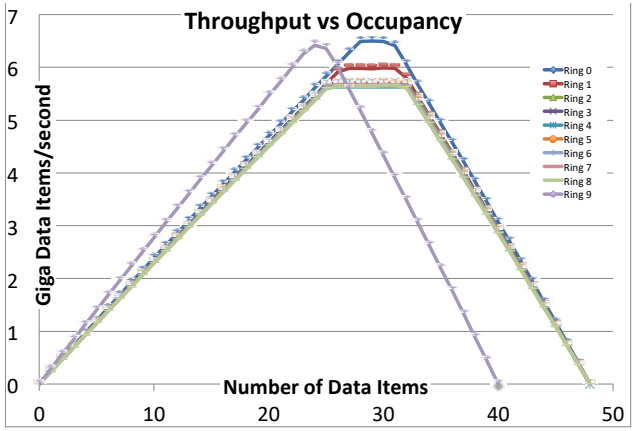
59



slide 60 of 67

60

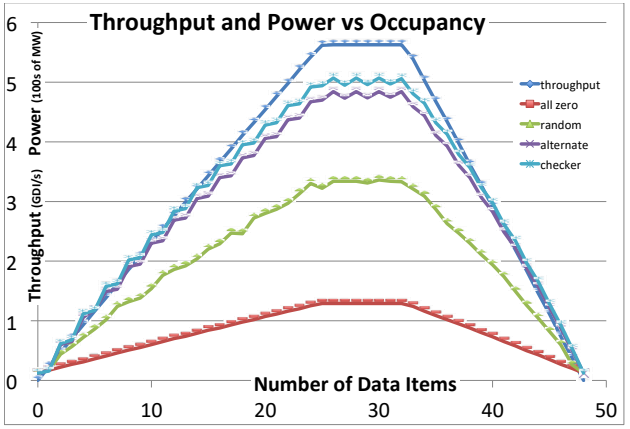
Performance without clocks (Weaver)



slide 62 of 67

62

Power versus Data (ring 3)



slide 65 of 67

65

References

for Link-Joint references, see: https://arc.cecs.pdx.edu/publications

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66

67