Syntax-directed translation

Rajit Manohar

Asynchronous VLSI and Architecture (AVLSI) Group Computer Systems Lab, Yale University

https://csl.yale.edu/~rajit/
https://avlsi.csl.yale.edu/act



Yale

A direct path from CHP to gates

- Goal: to provide a direct path from CHP to gates
- "Syntax directed"
 - Translation uses the syntax of the CHP program to generate the circuit
 - Uses structural induction
 - Induction on the structure of the program
 - Translations for
 - Base case: assignment, communication, skip, expression evaluation
 - Induction: selections, loops, sequential composition, parallel composition
- History

b

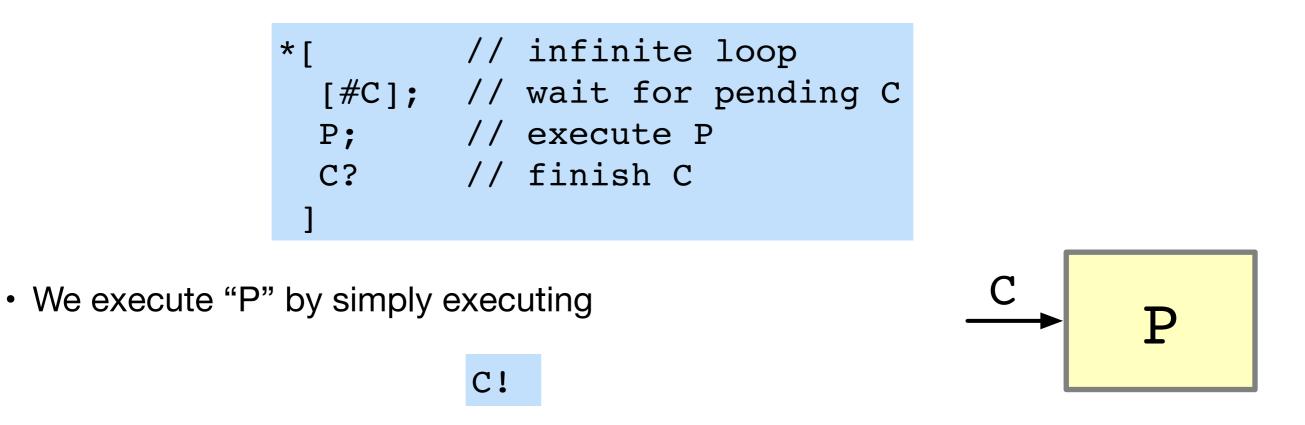
- * 1988 : paper at Conference on Advanced Research in VLSI (Caltech)
- * 1991 : Tangram language / Haste @ Handshake Solutions (Philips Research)
- * 1998 : Balsa, based on Tangram with extensions (U. Manchester)



Key idea

Zale

- Use a communication *channel* to select a program for execution
- Given a program "P", we will implement the following

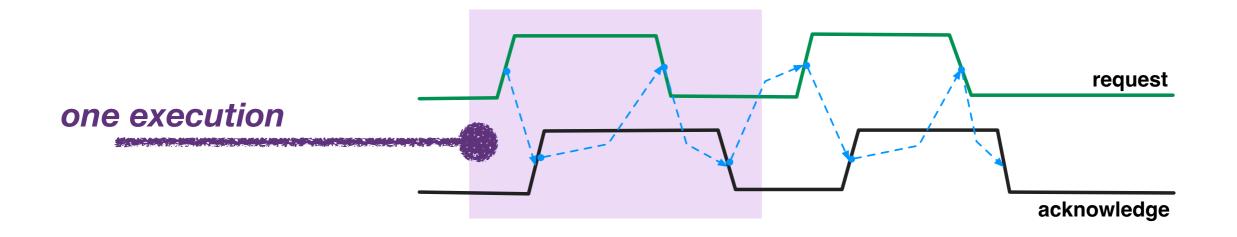


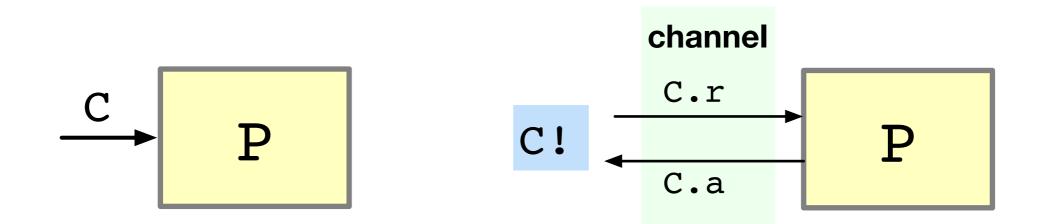
• This is sometimes called "process decomposition" or "process call"



Wire implementation of channels

• Channel "C" that *controls* the execution of a program



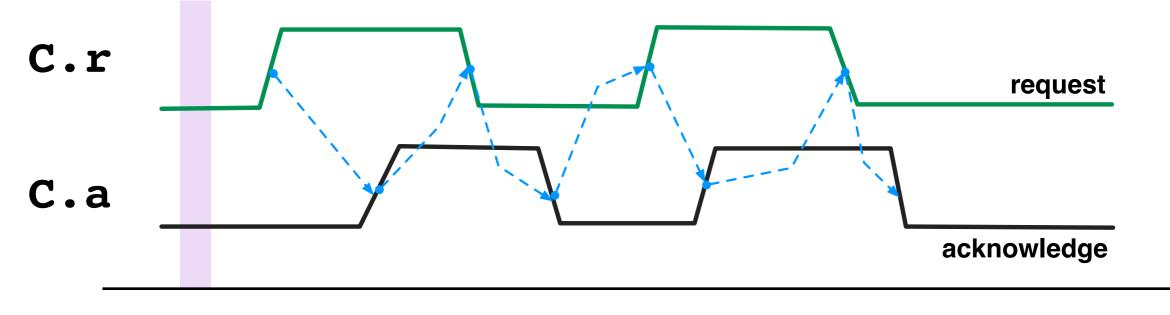


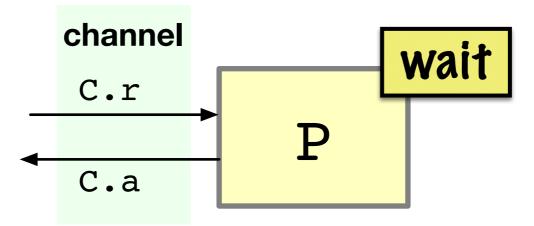




One execution: idle (waiting) state

Yale

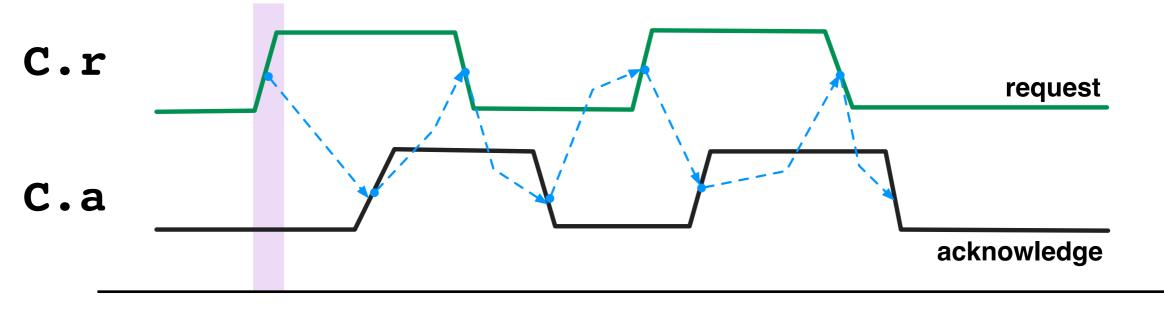


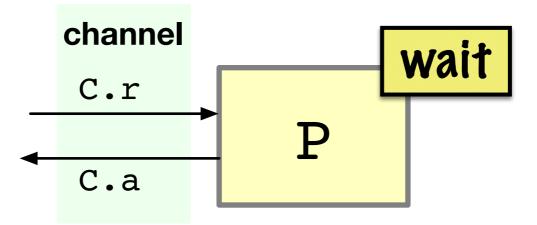




One execution: request execution

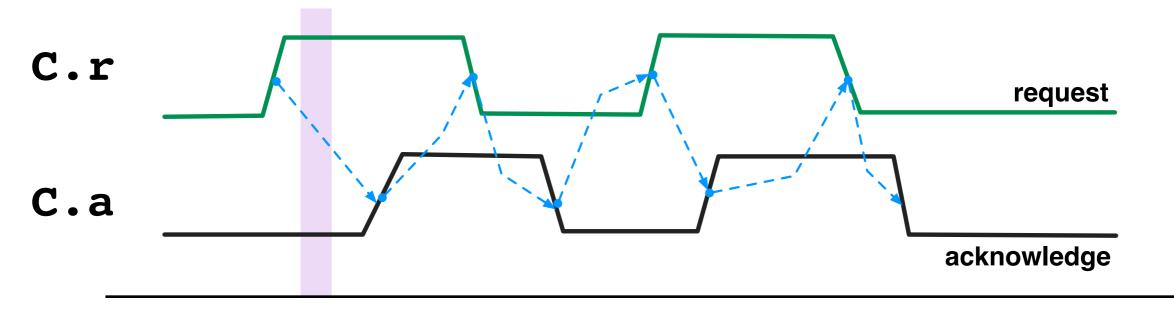
Yale

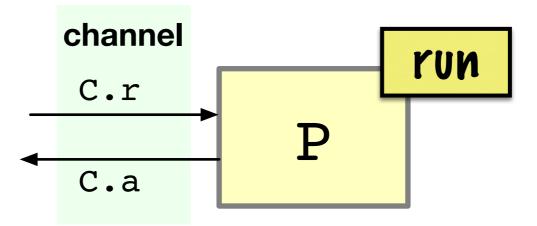






One execution: running

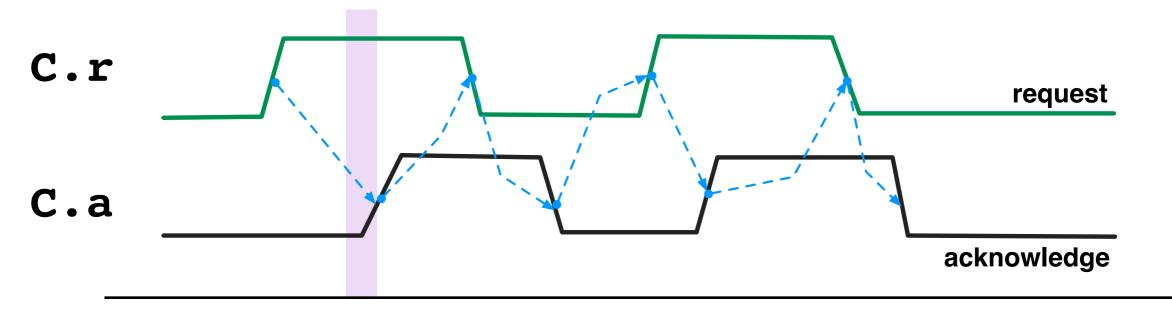


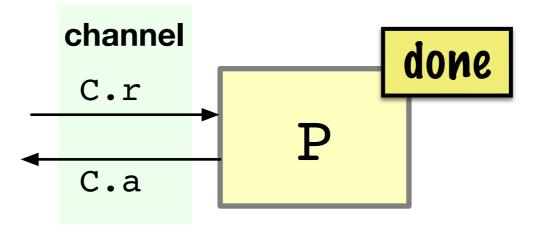






One execution: done

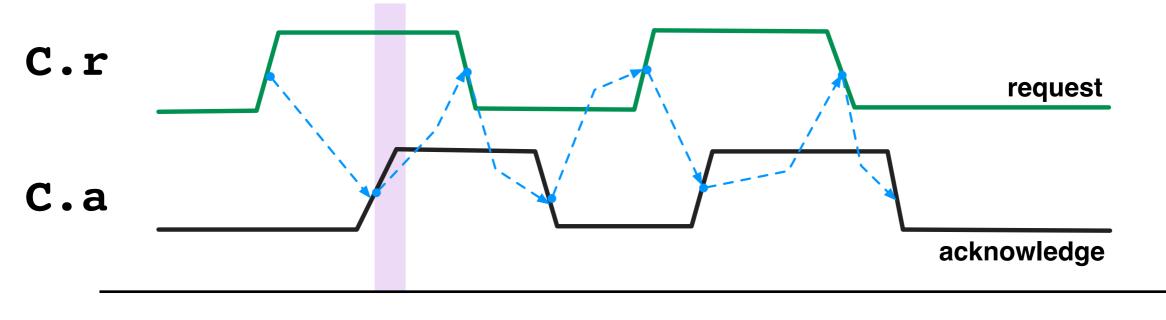


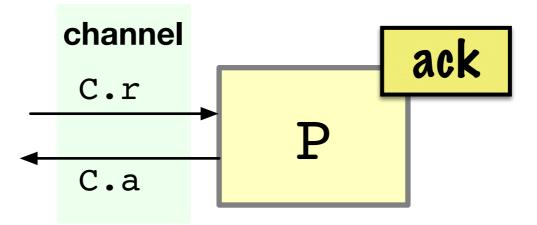






One execution: respond to requester

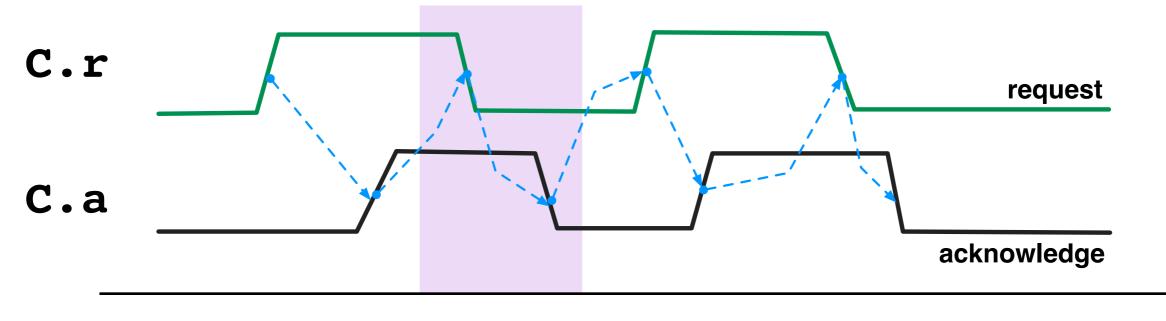


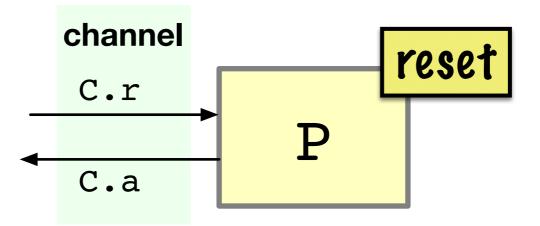






One execution: reset phase



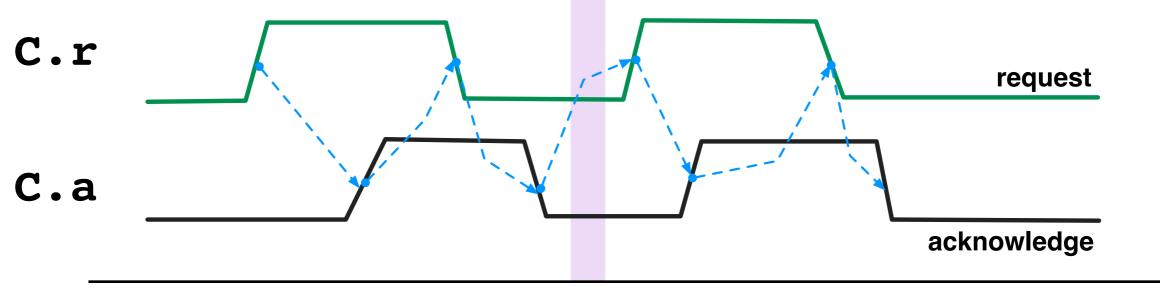


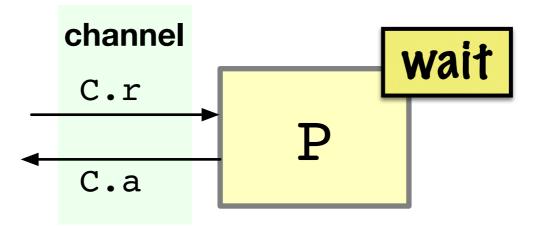




One execution: reset phase

Yale







Variables

- Two operations
 - Write a value to the variable

W!value



* Read the current value of the variable

R?x

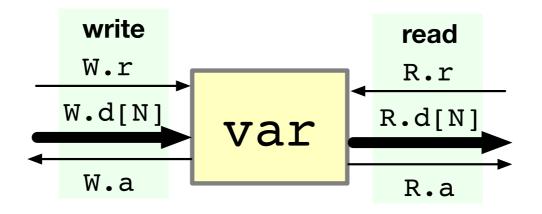
- The variable itself is "passive"
 - * It waits for the environment to either write or read its value

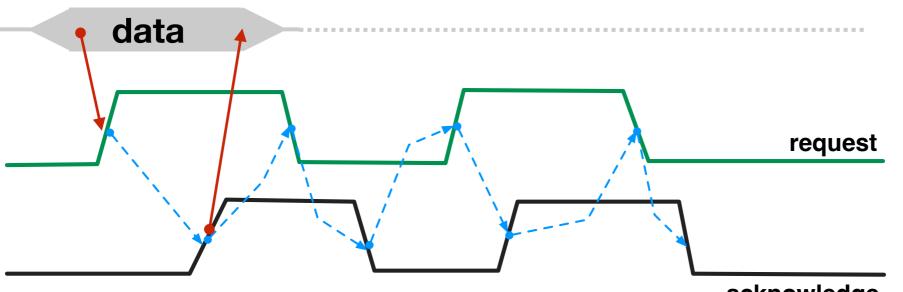




Writing and reading a variable

Yale



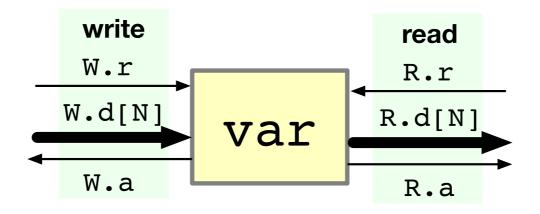


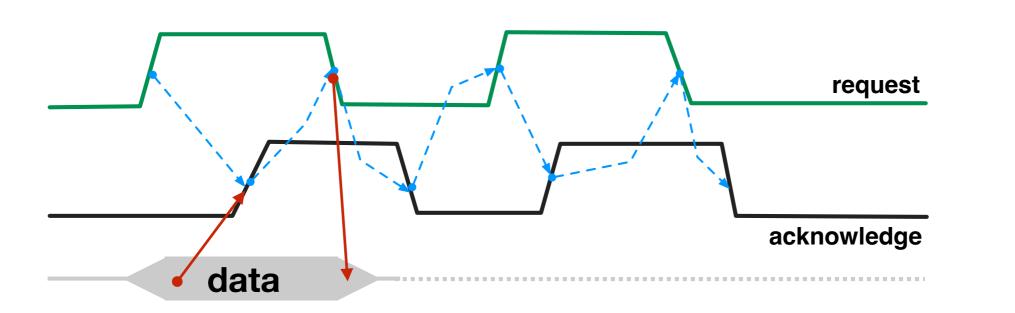
acknowledge

AVLSI

Write

Writing and reading a variable



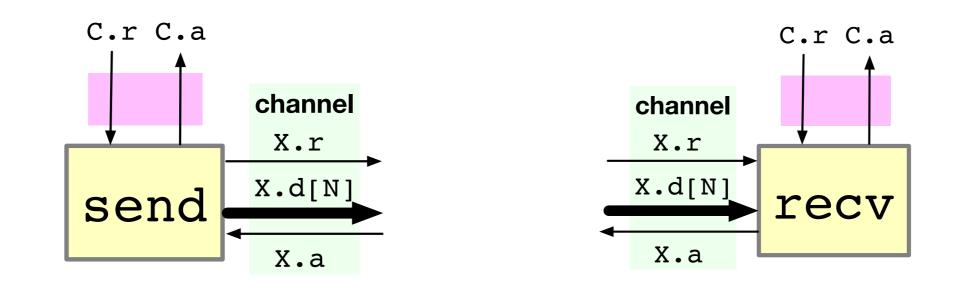


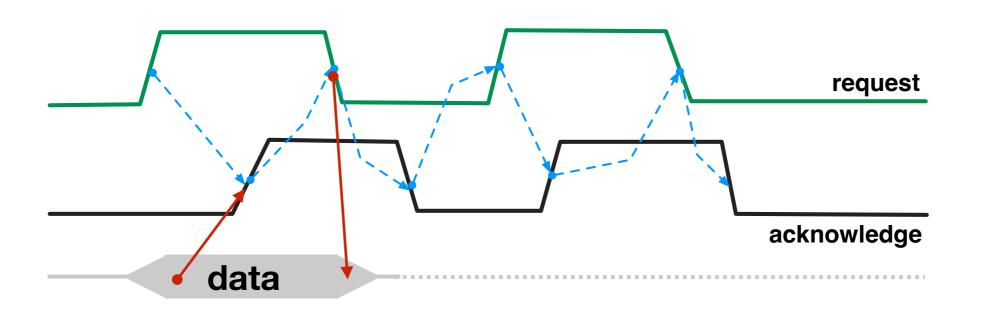


Read

Yale

Sending and receiving on a channel



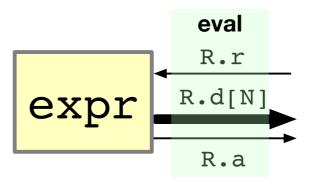




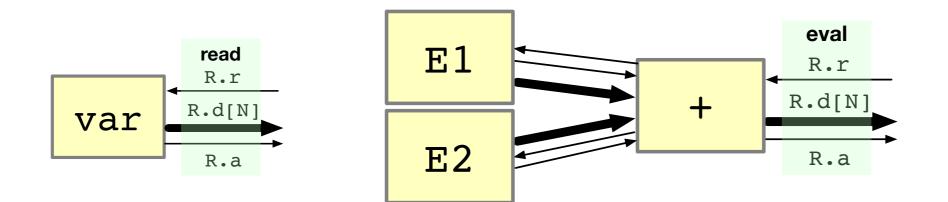
Send / receive

Yale

Expression evaluation



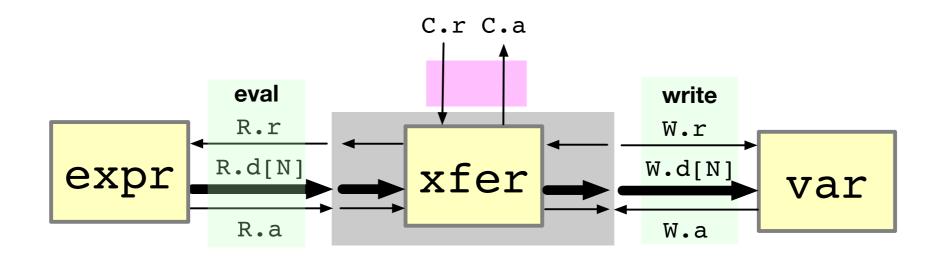
• Example of expression de-composition







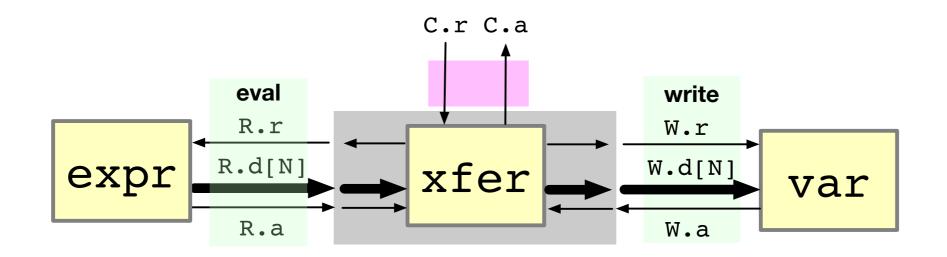
Assignment

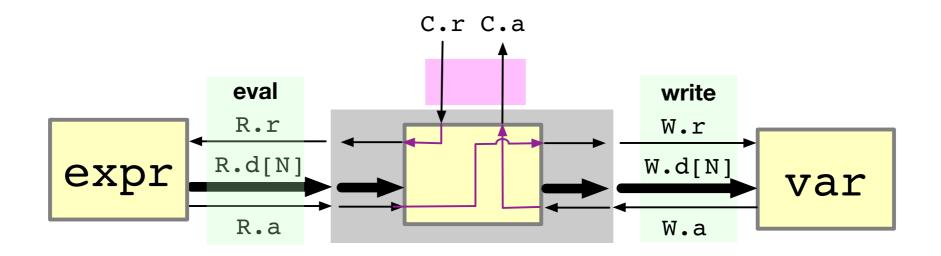






Assignment

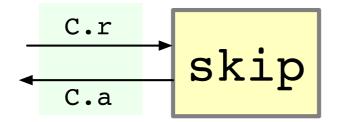


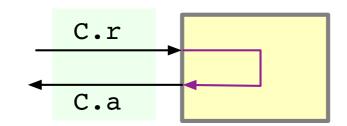






Building blocks

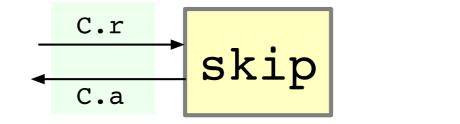


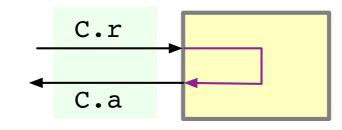


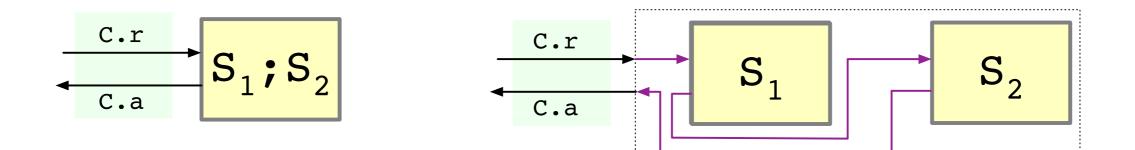




Building blocks



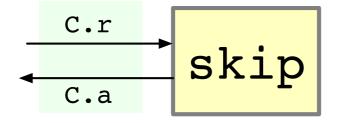


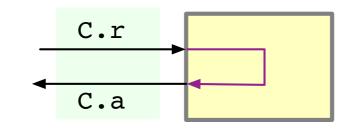


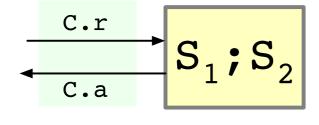


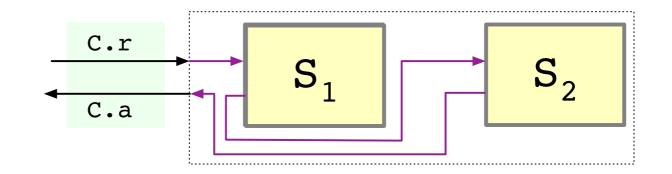


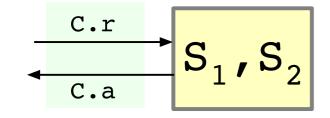
Building blocks

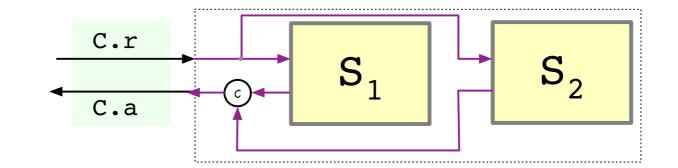








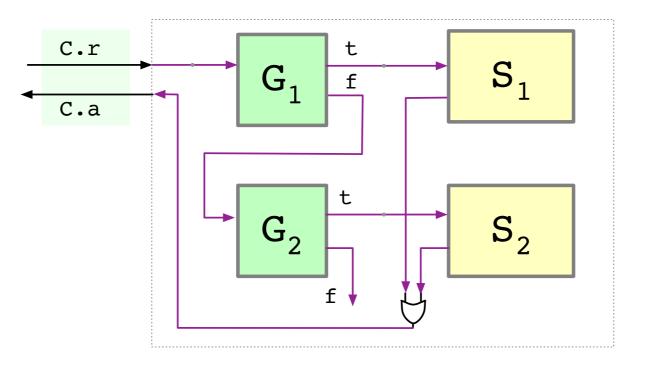


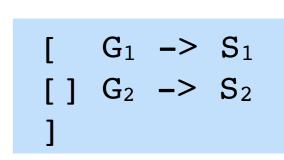




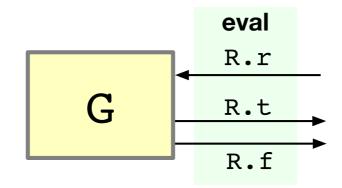


Selections and loops





Selection

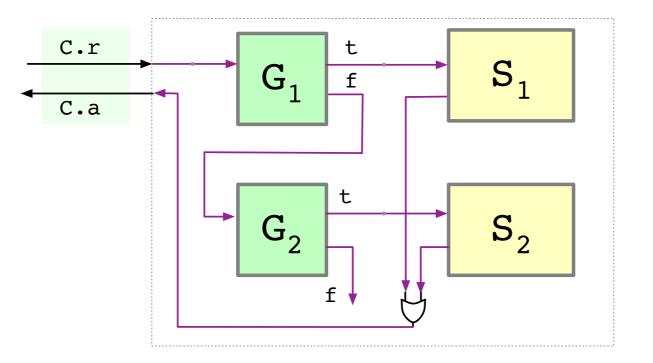






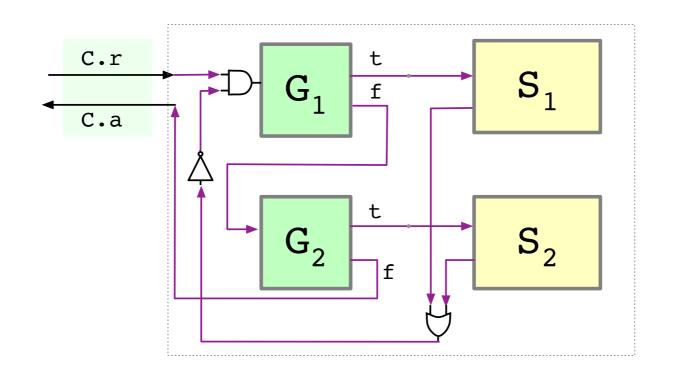
Selections and loops

Yale



$$\begin{bmatrix} G_1 & -> & S_1 \\ G_2 & -> & S_2 \\ \end{bmatrix}$$

Selection



Loop

