

# Gates and gate-level design

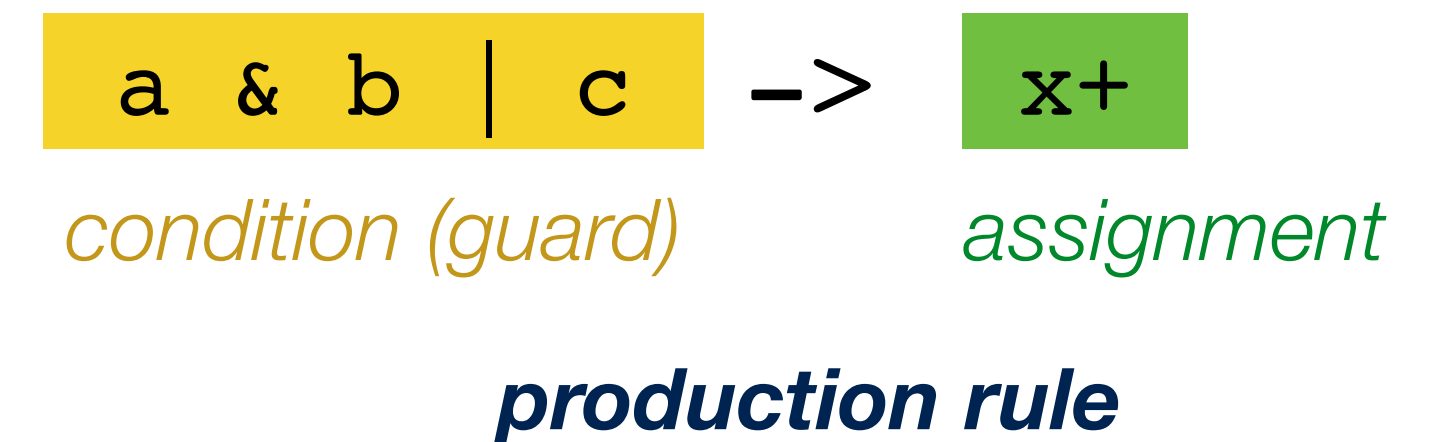
Rajit Manohar  
Computer Systems Lab  
Yale University



# Gate-level modeling

---

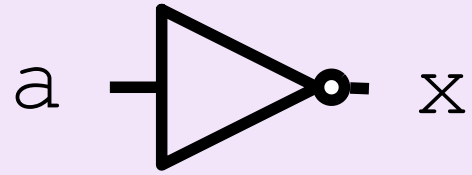
- Digital logic
  - ❖ All variables must be mapped into Booleans (0/1)
  - ❖ If we already have a Boolean variable, direct mapping
  - ❖ N-bit integers : use N one-bit variables
- Circuit often includes signal + complement
  - ❖ Sometimes made explicit by having two variables for a Boolean
- Gates manipulate Boolean values



# Writing gates in ACT

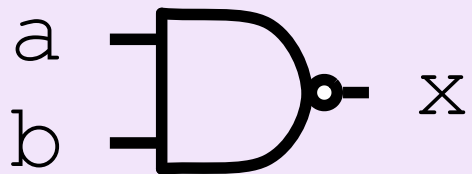
*short cuts*

**combinational**



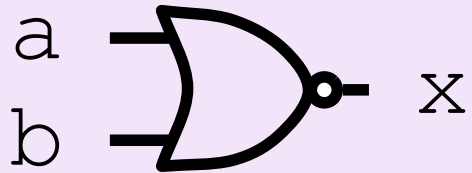
$a \rightarrow x-$   
 $\sim a \rightarrow x+$

$a \Rightarrow x-$



$a \ \& \ b \rightarrow x-$   
 $\sim a \ | \ \sim b \rightarrow x+$

$a \ \& \ b \Rightarrow x-$

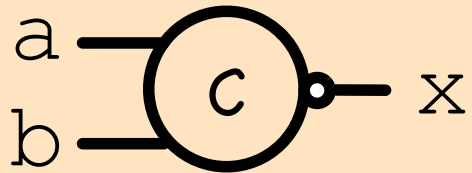


$a \ | \ b \rightarrow x-$   
 $\sim a \ \& \ \sim b \rightarrow x+$

$a \ | \ b \Rightarrow x-$

$\Rightarrow$   
 combinational  
 gate

**state-holding**



$\sim a \ \& \ \sim b \rightarrow x+$   
 $a \ \& \ b \rightarrow x-$

$a \ \& \ b \ \#\> \ x-$

$\#\>$   
 C-element  
 gate

```
bool a, b, c;

prs {
    a & b => c-
}
```

# A simple asynchronous circuit

- Two coupled oscillators
  - ❖ The C-element waits for the two inputs to agree

