Yale ENGINEERING

Gates and gate-level design

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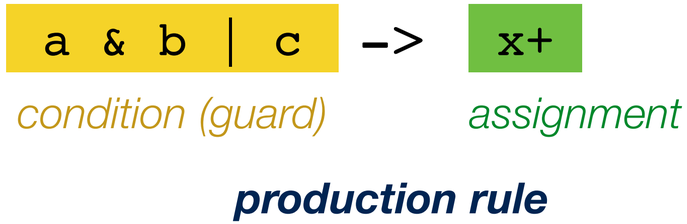
Gate-level modeling

- Digital logic
  - ❖ All variables must be mapped into Booleans (0/1)
  - ❖ If we already have a Boolean variable, direct mapping
  - ❖ N-bit integers : use N one-bit variables

- Circuit often includes signal + complement
  - ❖ Sometimes made explicit by having two variables for a Boolean

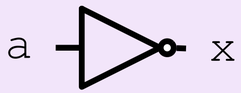
- Gates manipulate Boolean values



Writing gates in ACT

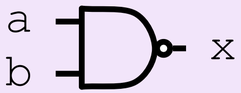
short cuts

combinational



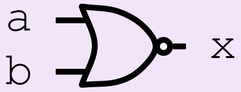

```
a -> x-
~a -> x+
```

```
a => x-
```




```
a & b -> x-
~a | ~b -> x+
```

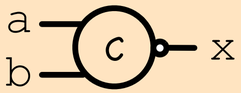
```
a & b => x-
```




```
a | b -> x-
~a & ~b -> x+
```

```
a | b => x-
```

state-holding




```
~a & ~b -> x+
a & b -> x-
```

```
a & b #> x-
```

```
~a & ~b -> x+
a -> x-
```

=>
combinational gate

#>
C-element gate

```
bool a, b, c;

prs {
   a & b => c-
}
```

A simple asynchronous circuit

- Two coupled oscillators
  - The C-element waits for the two inputs to agree