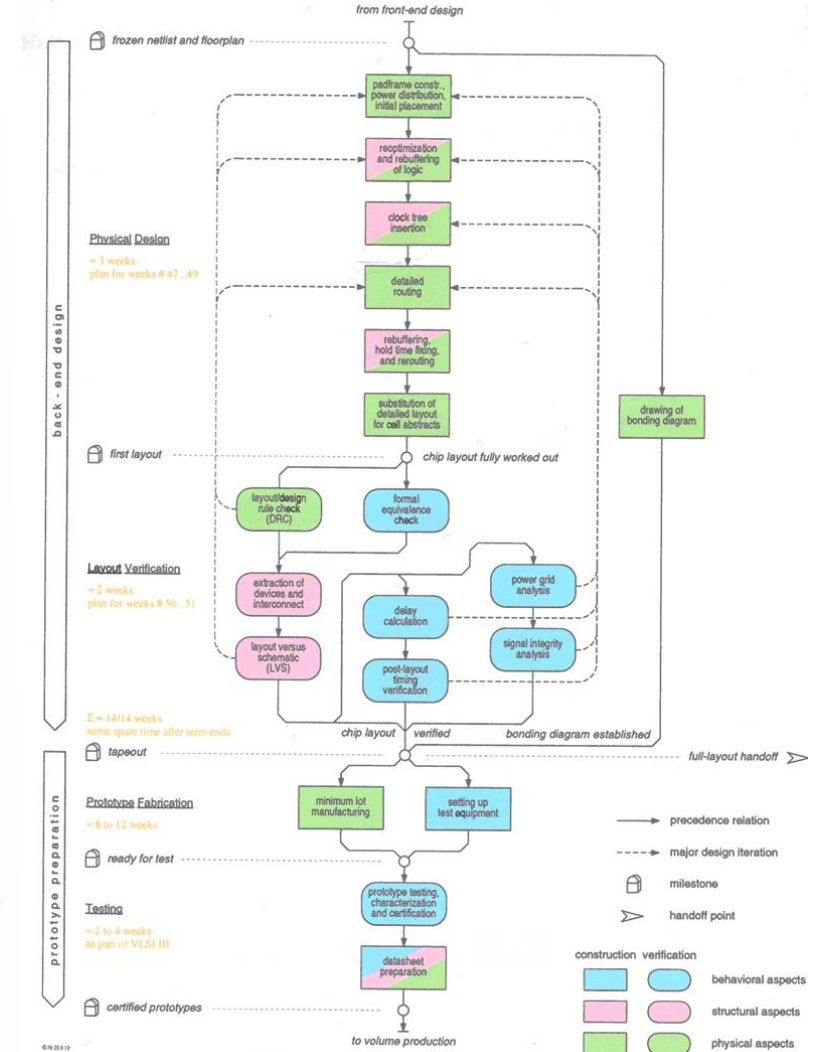
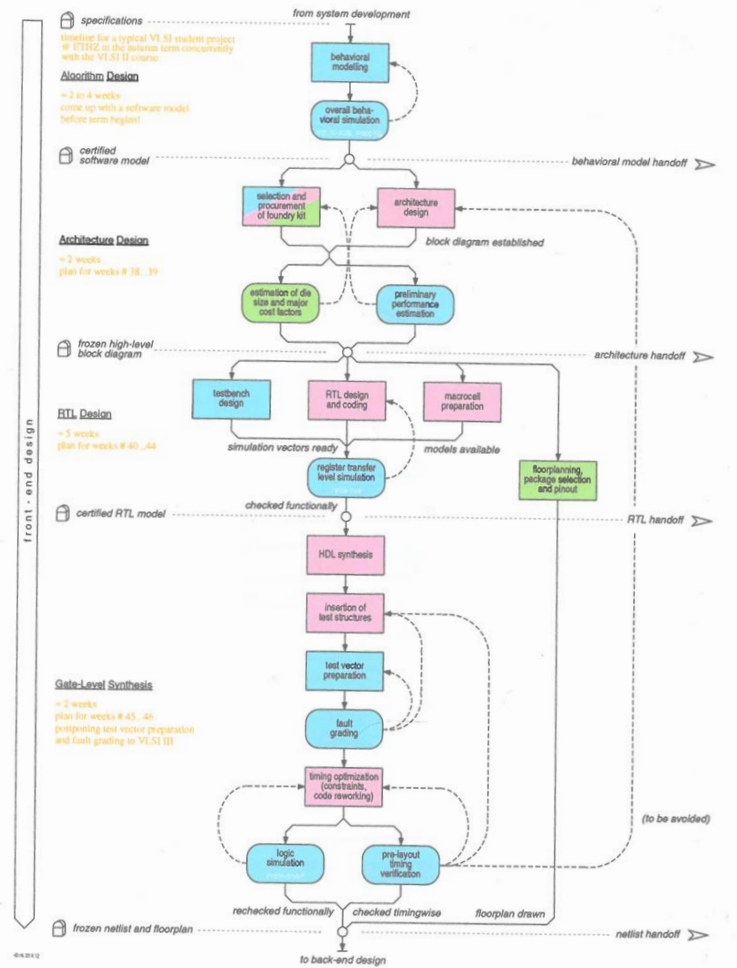


Ole Richter & Rajit Manohar

ASIC implementation flow

Why is ASIC design scary

- No trail and error
- Every miss step can be fatal
- Physics is out to get you
- Risk management
- A simulation is an abstraction



[H. Kaeslin 2015]

And why you should not be scared, but excited

- You are always a Team
- Tools are there to help check
- One rule to protect you:
“something not checked or verified is broken”
- Millions of designs have been fabricated

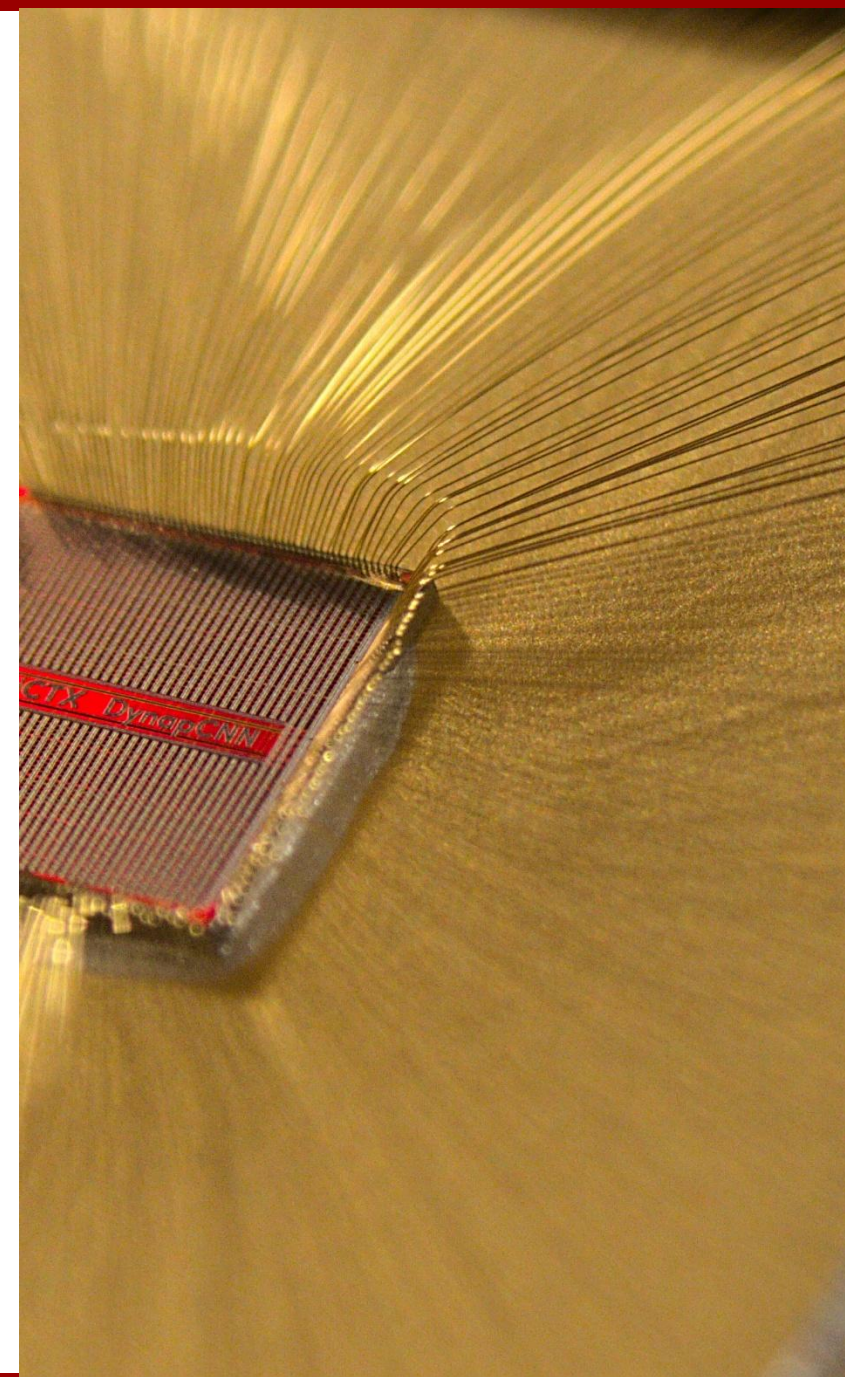
- You are building complex systems out of Atoms
- You are working with the most widespread and advanced human made technology
- (almost) everything depends on it (and you 😊).

Some Basics: ASICs

- Integrated Circuits (IC)
- Application Specific Integrated Circuits (ASIC)
- Complementary Metal Oxide Semiconductor (CMOS)
- Field Programmable Gate Array (FPGA)

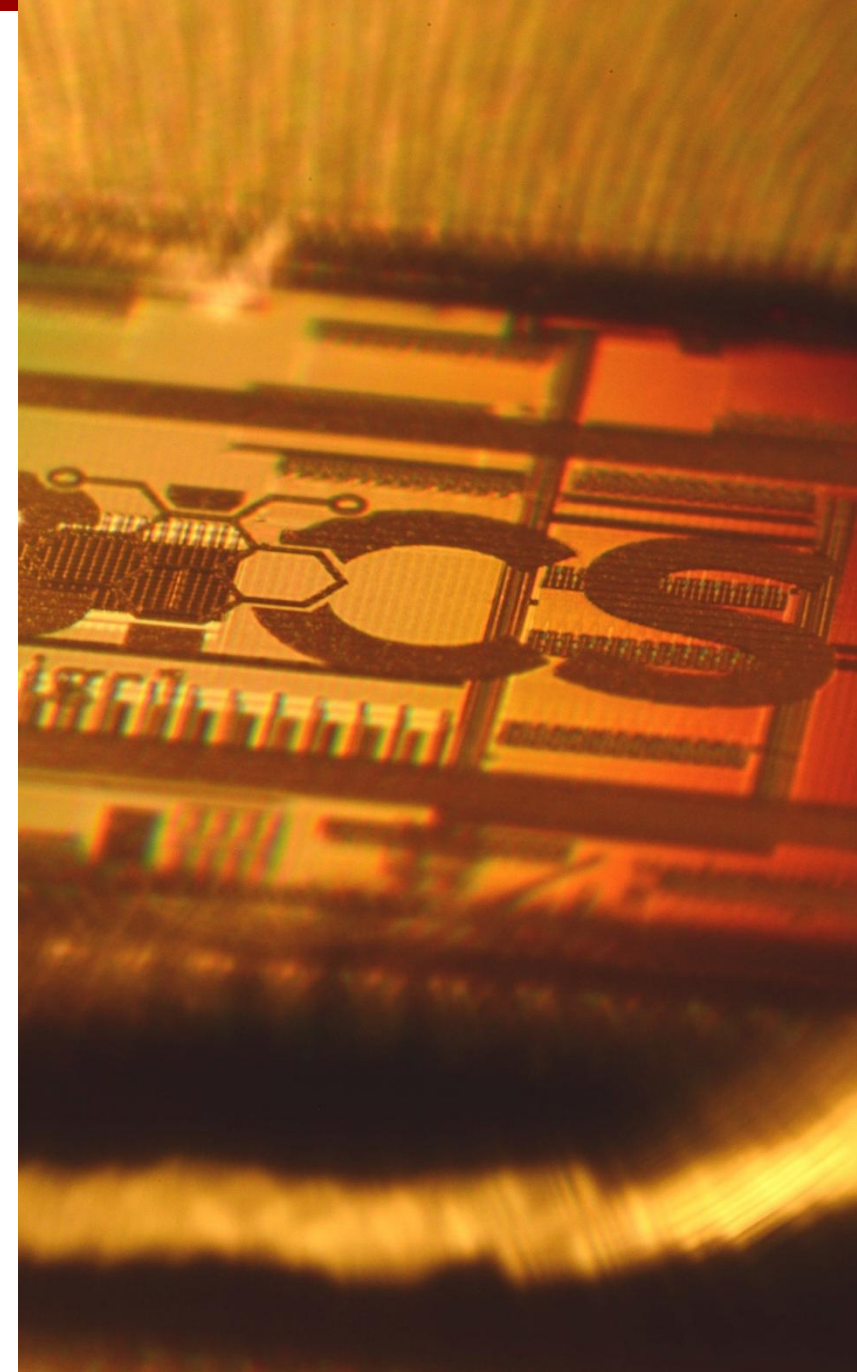
Other Variants:

- Very Large Scale Integration (VLSI)
- Programmable Logic Array (PLA)



Some Basics: Cell libraries

- Set of preprepared compact Elements
- Logic
- State-holding



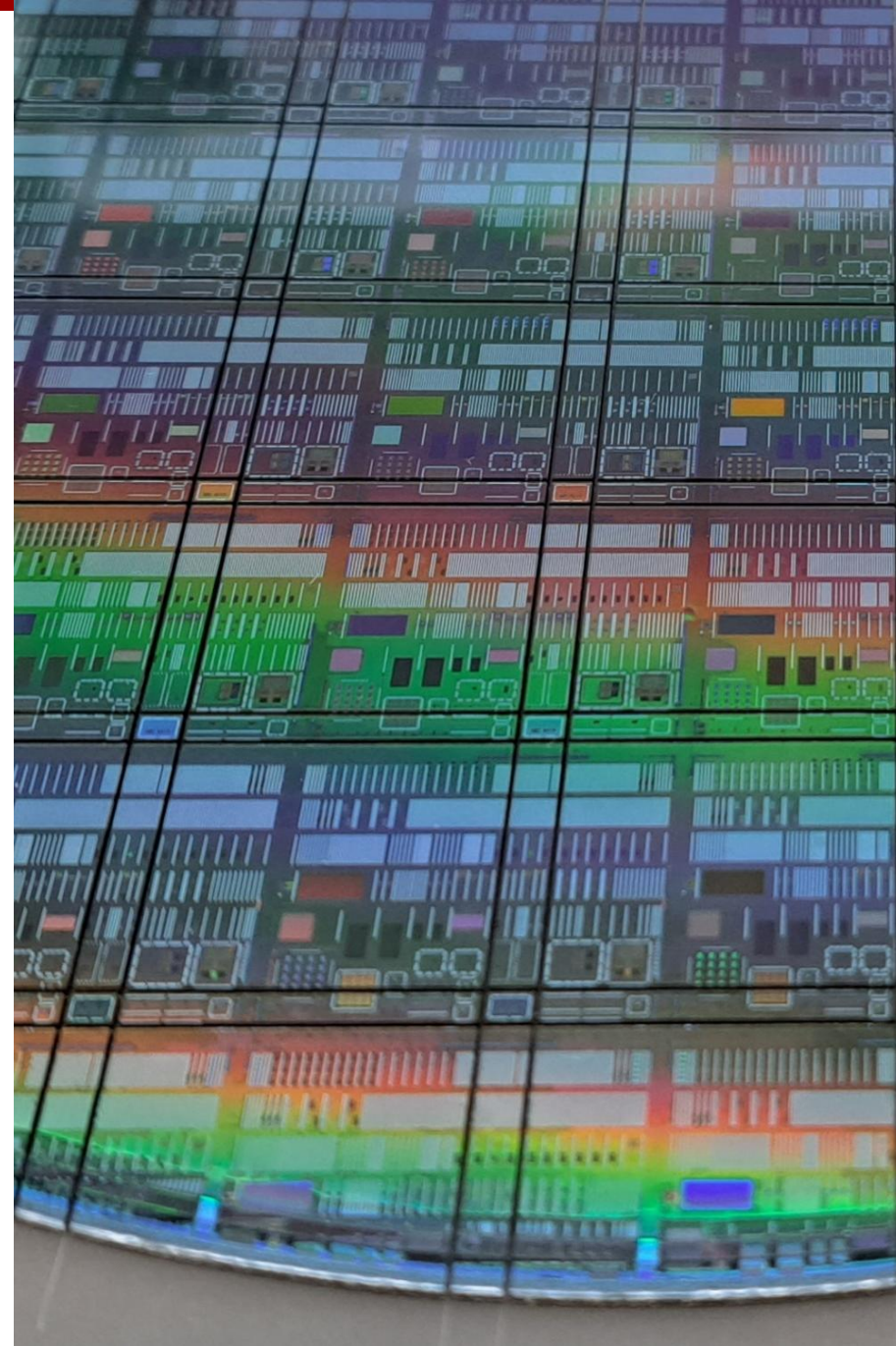
Synthesis and Cell Mapping

- Take your PRS to a specific technology
- Fan-out

- Building functionality out of given elements

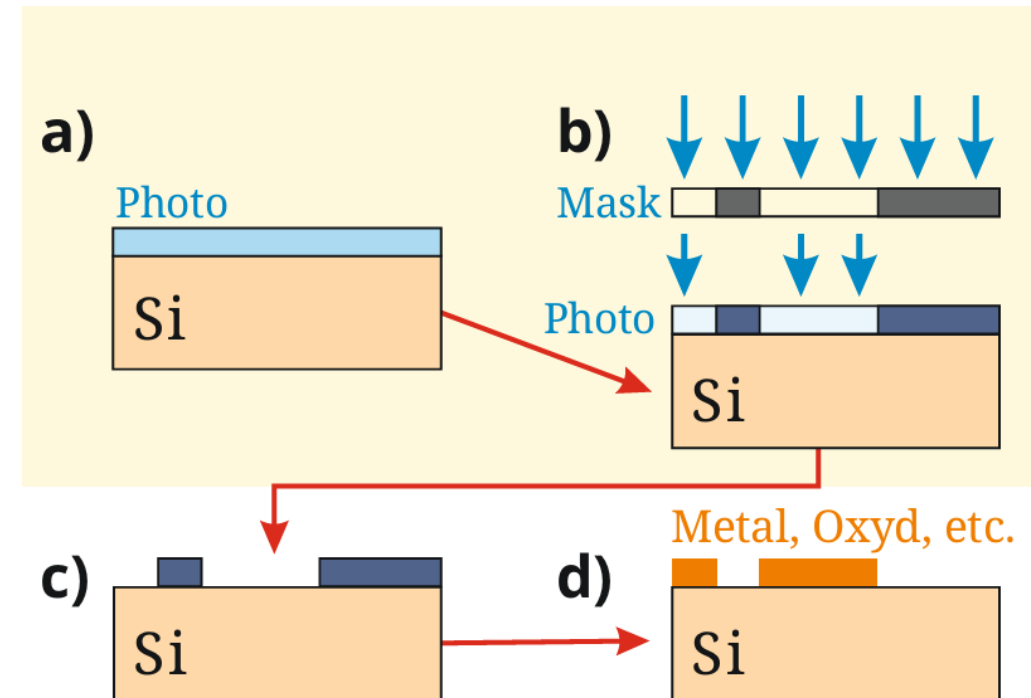
Things to watch out for

- Make sure the synthesized result still does what you want it to do
- Verify it, as this becomes the reference that all further steps are checked with!
- Something that is not verified is broken.
- Check warnings. Tools don't work magic.



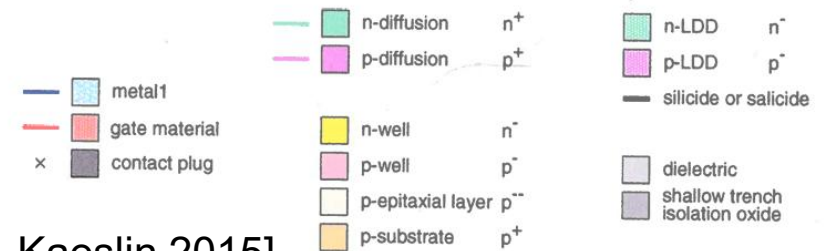
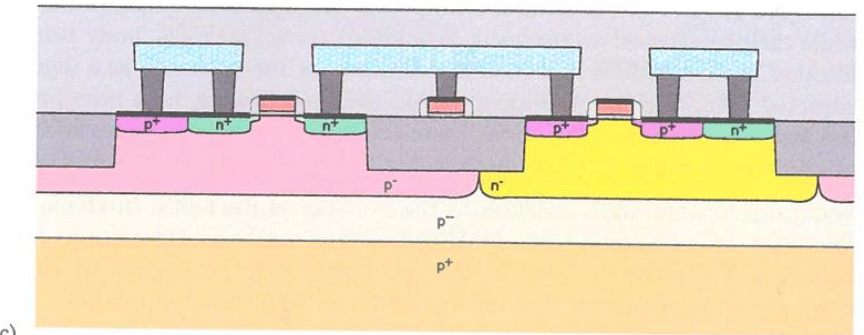
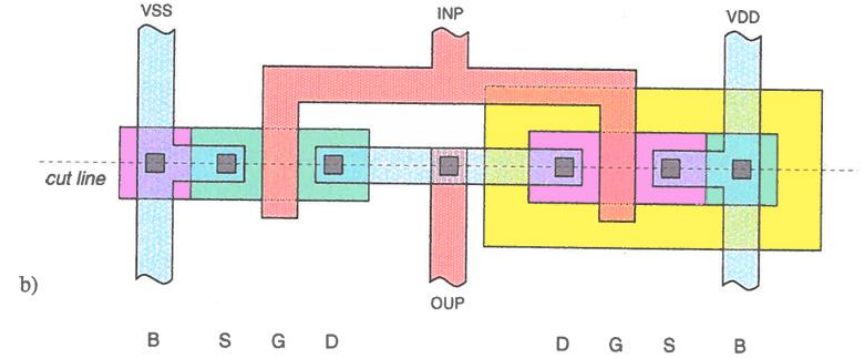
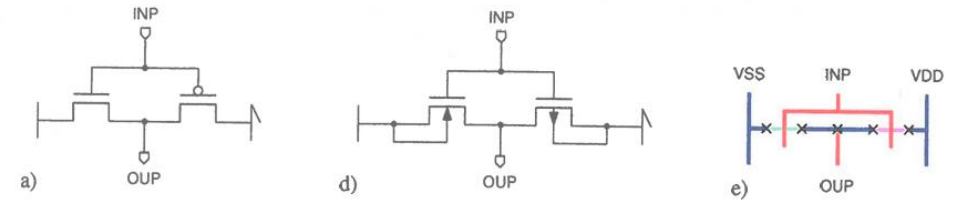
Some Basics: CMOS Technology

- Lithography
- Layer by layer
- Single crystal Si



Some Basics: Layout

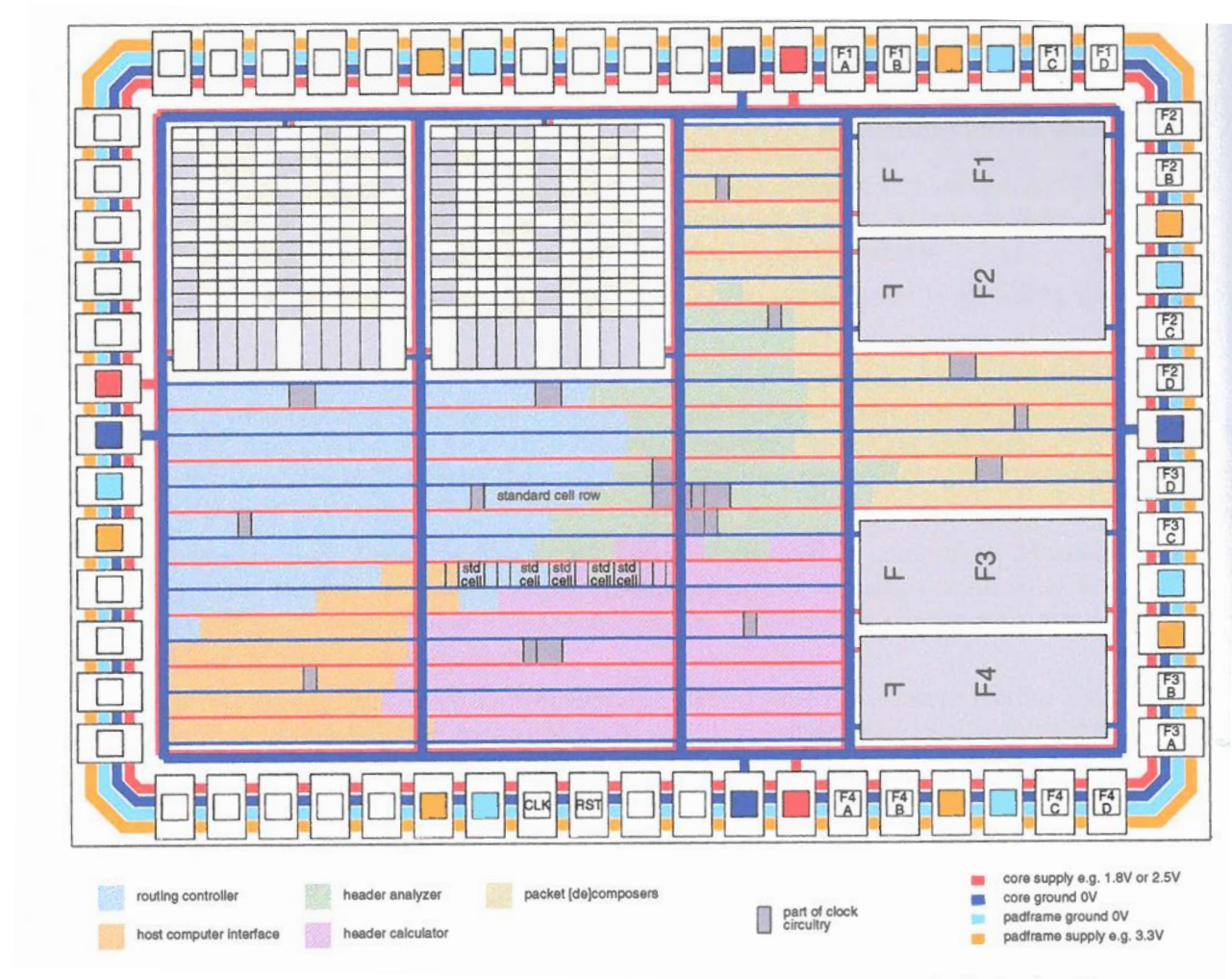
- Drawing rectangles
- Function by different sets of shapes
- Top down view



[H. Kaeslin 2015]

Floorplan

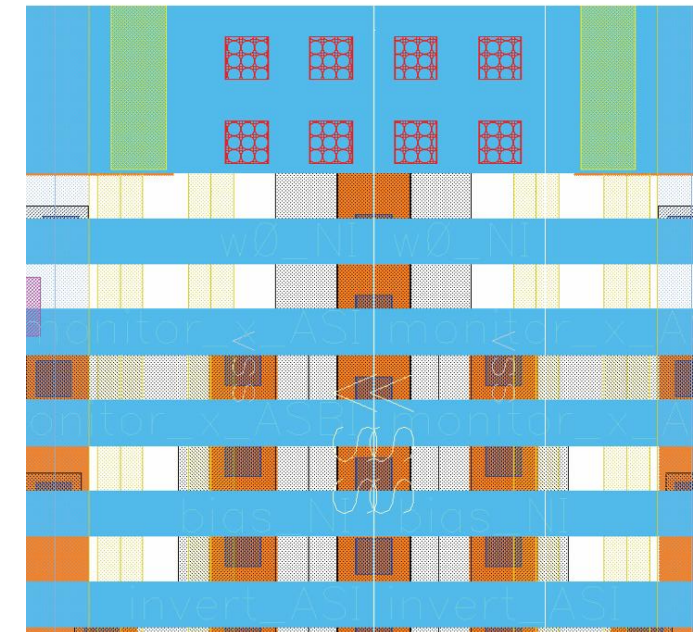
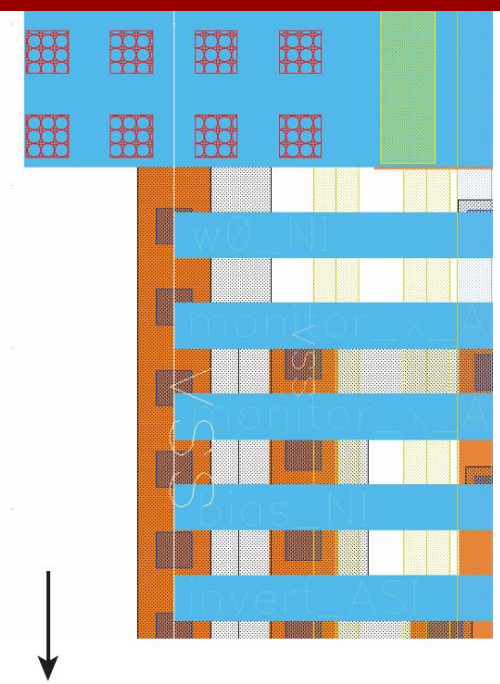
- Where to place what
- > Layout -> lef, cells
- > PhyDB -> def
- > Dali -> PhyDB (def)



[H. Kaeslin 2015]

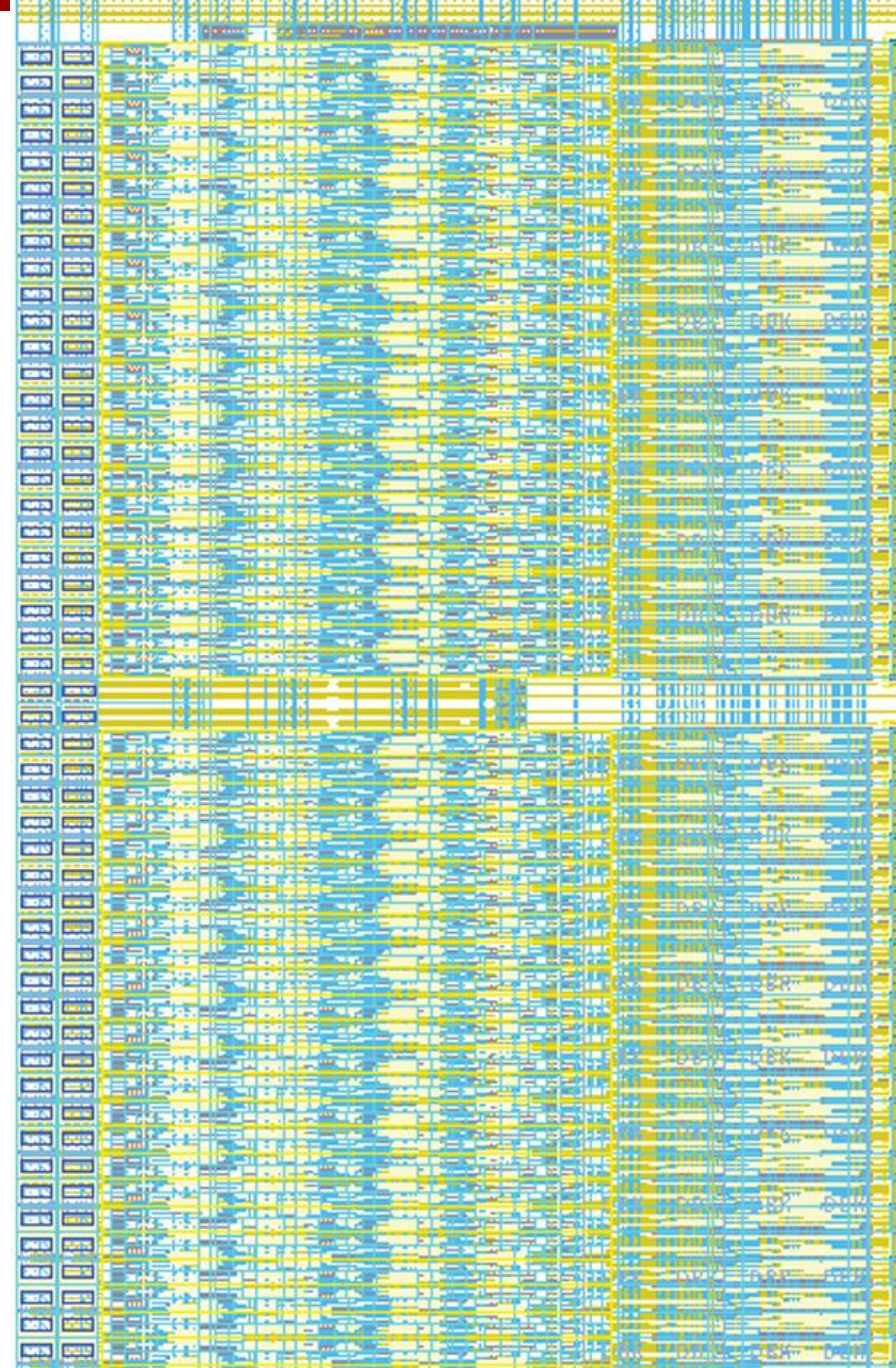
Standard Cells, Macros and Tiling

- Puzzle
 - Grid vs track
 - Matching Libraries
 - Predesigned
-
- > Jigsaw



Placing the cells

- Place all your logic cells
 - With minimum connection distances
 - Cells of the same function close
-
- > Dali



Demo

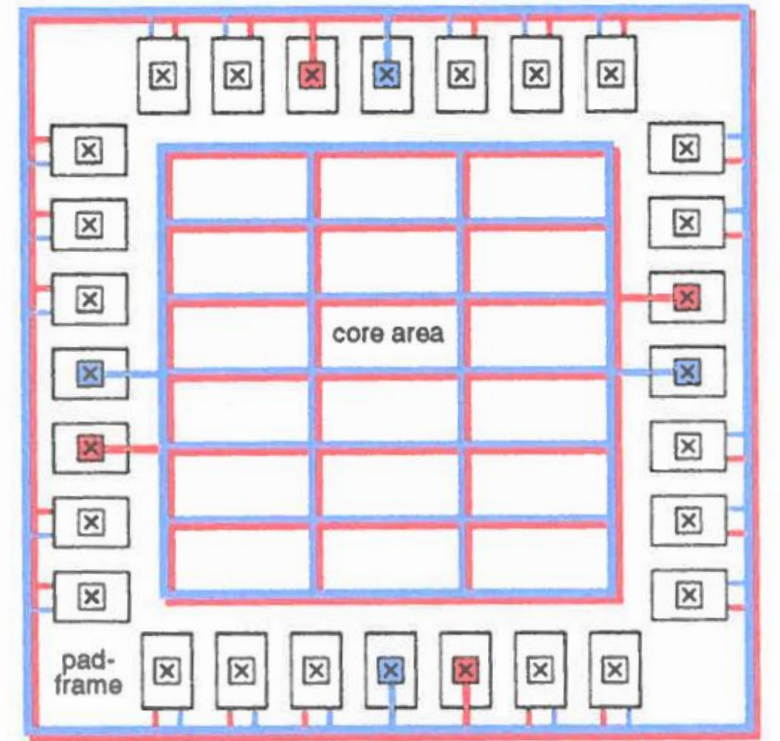
Some Basics: Padframe and I/O

- The connections to the outside
- Amplifiers / Buffers
- Drive strength
- LVDS
- Structural Integrity



Power distribution and decoupling caps

- Energy distribution
- IR-drop
- Supply-bumps
- > SProute -> PhyDB (def)
- > PWroute -> PhyDB (def)

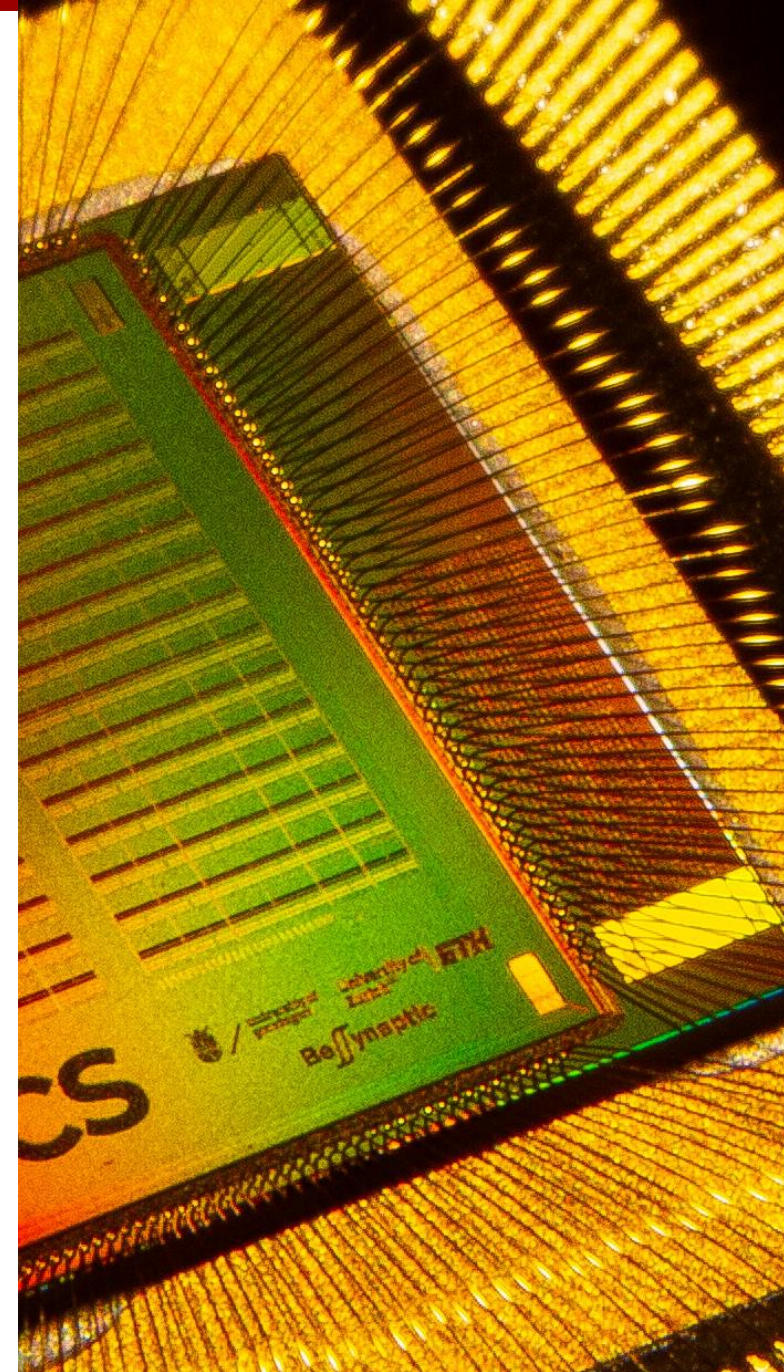


d) two metals separate supplies peripheral pads

[H. Kaeslin 2015]

Routing

- Connect all the wires
 - Connect power
 - Double cut
 - Shielding
 - To dense
 - Antenna
-
- > TritonRoute WXL or commercial tools



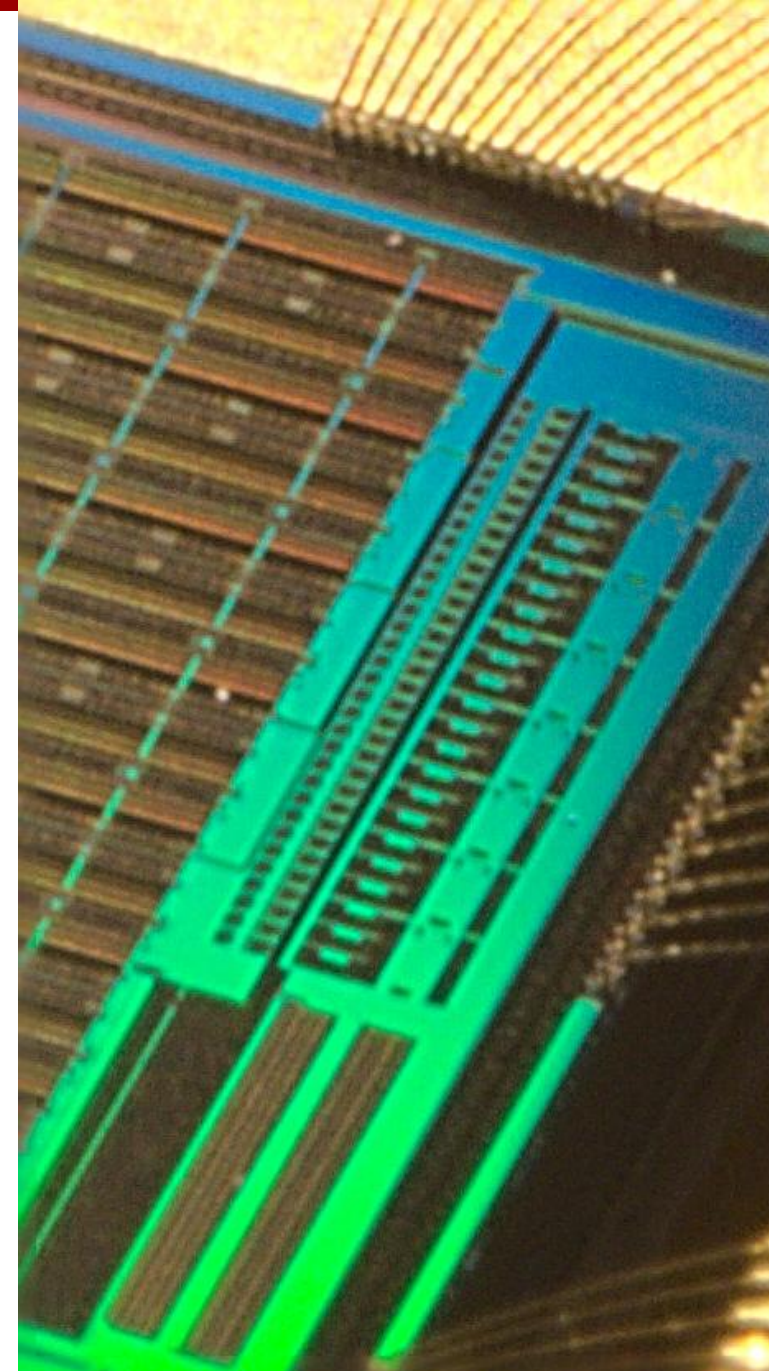
Demo

Parasitics

- Between lines of the same metal
- Between lines of different metals
- Between metal and substrate
- FET
- Line and sheet resistance
- Via resistance
- Poly resistance

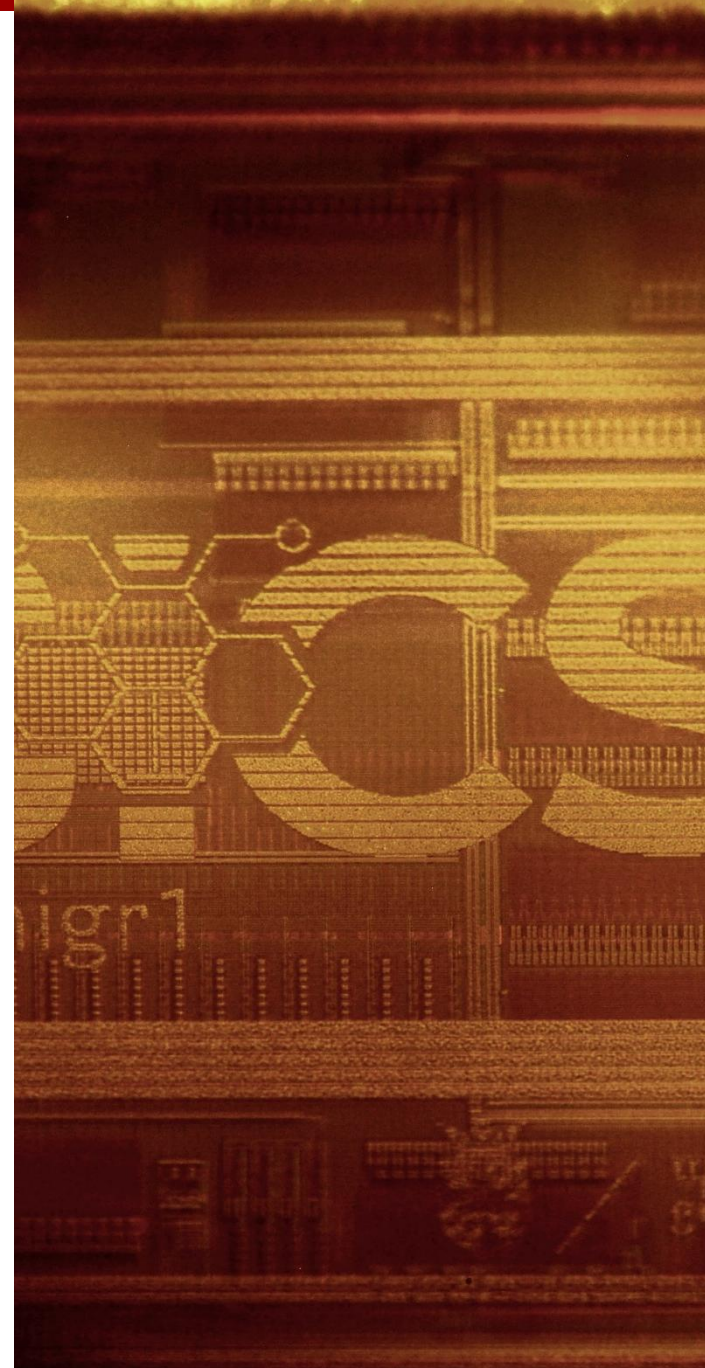
Parasitic Extraction

> SPEF to back annotate ActSim, Cyclone as well as your Spice!



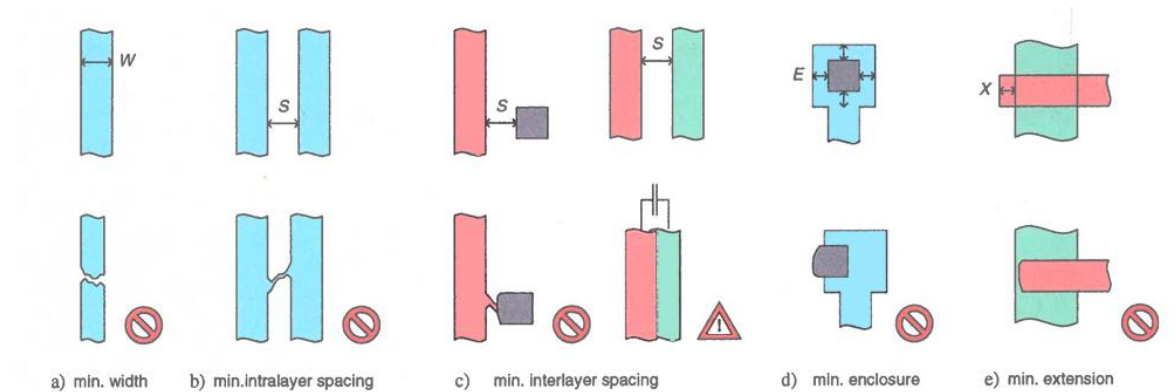
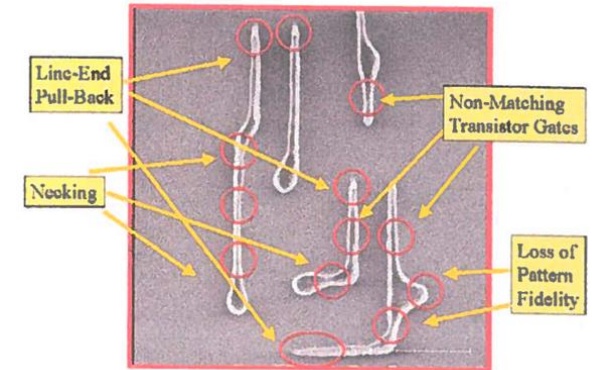
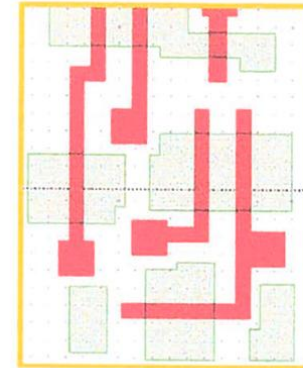
Physical Verification

- DRC
- LVS
- DFM



Design Rules

- Rules for producible designs
- Memory rules
- Do not violate them
- Do not waive them
- They are there to protect you (and the foundry)



[H. Kaeslin 2015]

Sometimes starting new is quicker than fixing

Don't give up, be stubborn and pull through

Something not verified is broken