EENG 426/CPSC 459/ENAS 876
Silicon Compilation

Well plugs. Pads

Computer Systems Lab

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Fall 2018

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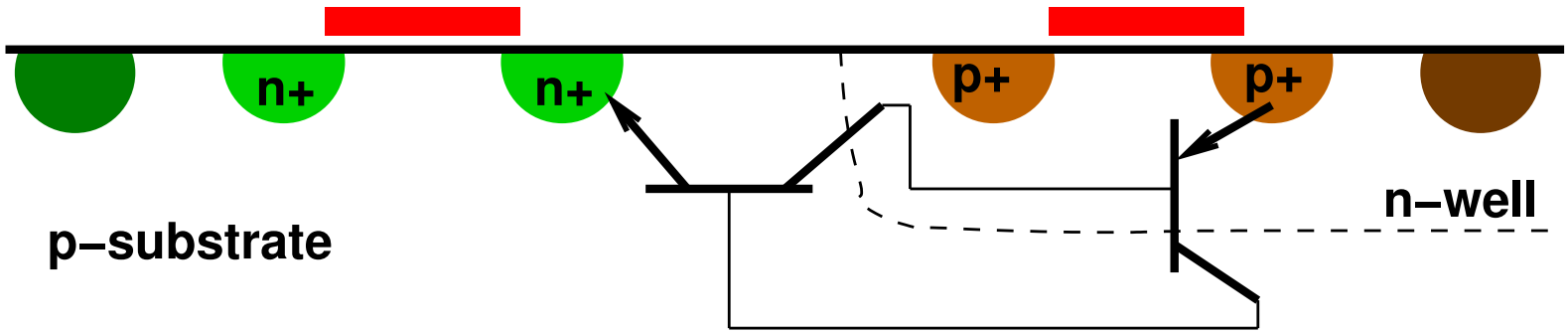
Wells

CMOS latchup



Well contacts prevent this pair from turning on.

Wells

- `magic` generates wells automatically
  - ... by bloating the diffusion region
- Try `:cif see CWP` or `:cif see CWN`
- *p*-type transistors in *n*-type well (connected to `Vdd`)
- *n*-type transistors in *p*-type well (connected to `GND`)
- Use *substrate* (*well*) contacts
  - Contacts: `psc`, `nsc`

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Chip I/O

To get signals on and off a chip:

- *Pads*: big metal "sandwich"
- Input/output pins on the chip are bonded to pads
- Wires from layout connected to pads
- Pad design rules don't scale
  (bonding machines constrain them)

Organization:

- Periphery of chip
- Multiple layers
- Array pads

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Pads

Multiple types:

- Input pads
- Output pads
- Bidirectional pads
- Tristate pads

Others:

- Power supply pads
- Level shifting pads
- Analog (bare) pads
- LVDS pads, etc etc.

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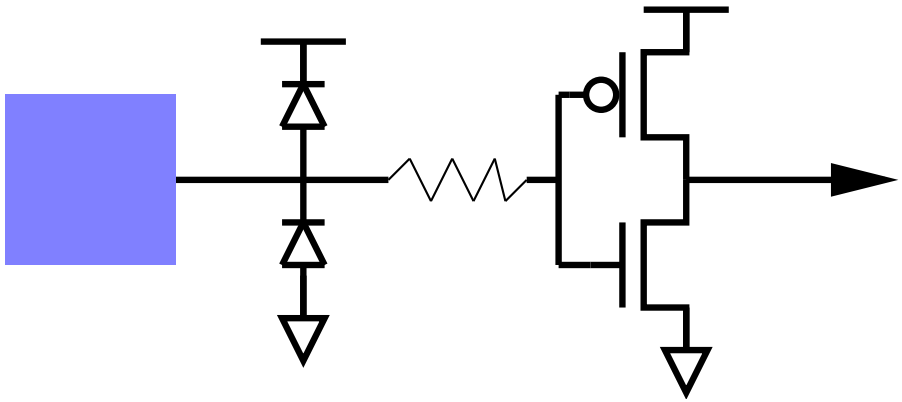
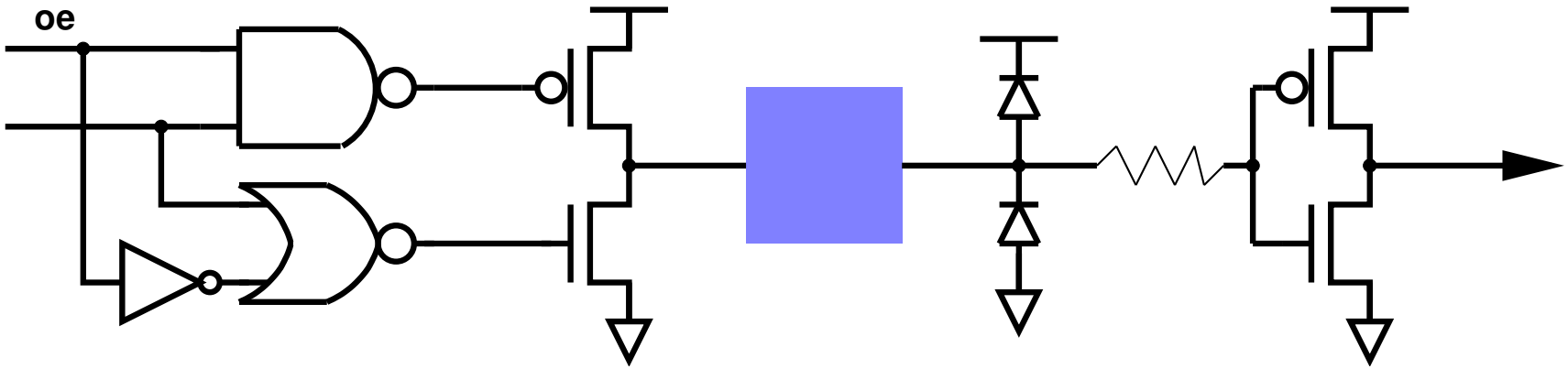
Input pads

What do we know about the inputs from off-chip?



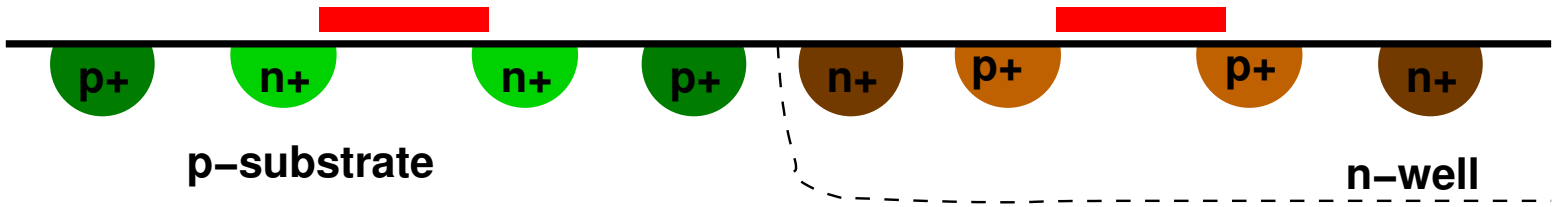
Bidirectional and tristate pads

Why do we use this particular structure?



Guard rings

Used to isolate sensitive parts of the circuit from "noisy" parts.



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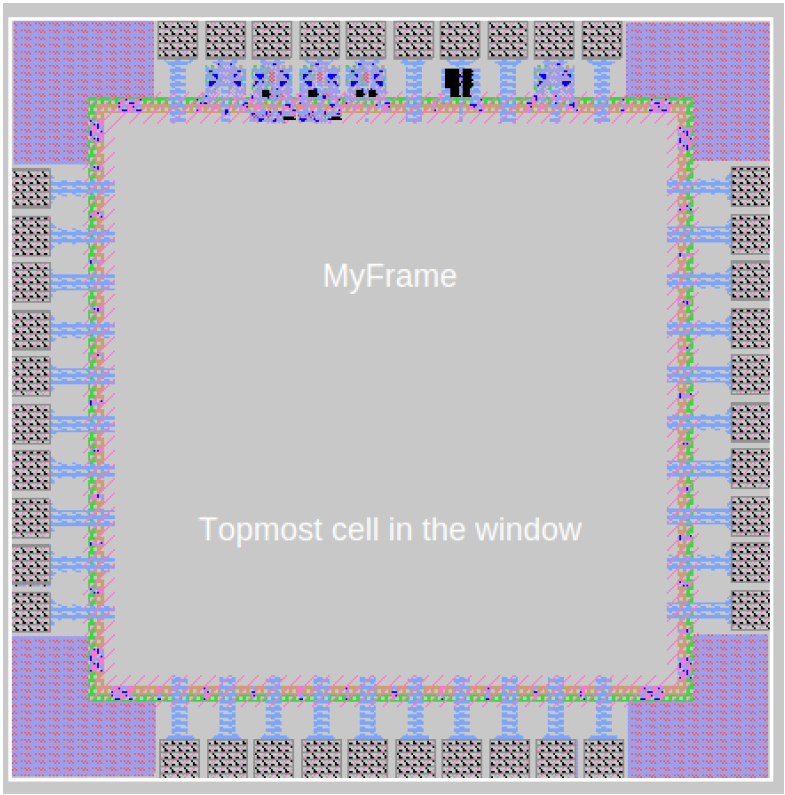
Pad frame



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