

# EENG 426/CPSC 459/ENAS 876 Silicon Compilation

## Syntax-directed translation

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Fall 2018

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## Syntax-directed translation

### Goal:

- Convert CHP program into production rules
- Translation will be
  - Correct
  - Inefficient except for the simplest examples

### Syntax-directed:

- Construction is by *structural induction* on the syntax of the CHP program

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## CHP summary

$x := E, \text{ skip}$

$S_1; S_2$

$[G_1 \rightarrow S_1 \parallel \dots \parallel G_n \rightarrow S_n]$   
 $[G_1 \rightarrow S_1 \mid \dots \mid G_n \rightarrow S_n]$

$*[G_1 \rightarrow S_1 \parallel \dots \parallel G_n \rightarrow S_n]$   
 $*[G_1 \rightarrow S_1 \mid \dots \mid G_n \rightarrow S_n]$

$S_1 \parallel S_2$

$X!e \ X?v$

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## Implementing communication

Synchronization with **handshaking expansions**.

### Four-phase handshaking:

$X : x\sigma\uparrow; [xi]; x\sigma\downarrow; [\neg xi]$   
 $Y : [yi]; y\sigma\uparrow; [\neg yi]; y\sigma\downarrow$

$X$ : *active* communication protocol

$Y$ : *passive* communication protocol

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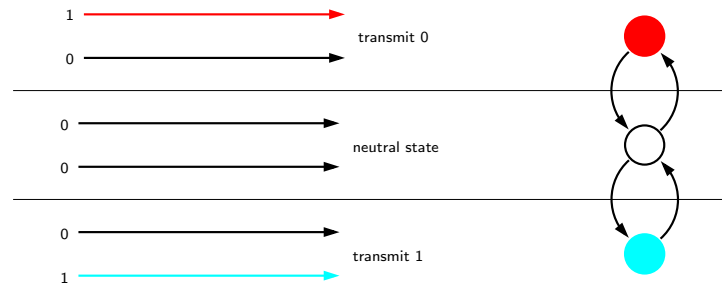
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## Implementing communication

Dual-rail encoding for data: a standard delay-insensitive (DI) code



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## Invariant

To run a statement  $S$ , we will assume:

- Input *control* channel  $C$
- Channel consists of two wires ( $ci$ ,  $co$ )
  - When  $ci$  goes high,  $S$  can start
  - When  $S$  is finished,  $co$  goes high
  - ... and the four phase handshake is finished

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## Invariant

To evaluate a one-bit expression, we assume:

- Input *control* wire
- A dual-rail output that specifies the value
- Variables will have a dual-rail value
- Expressions will be built using structural induction

(Primitives: AND, OR, NOT, variable)

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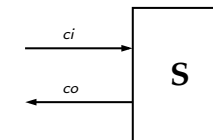
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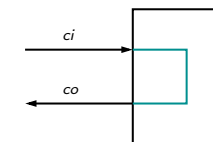
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## Translating skip



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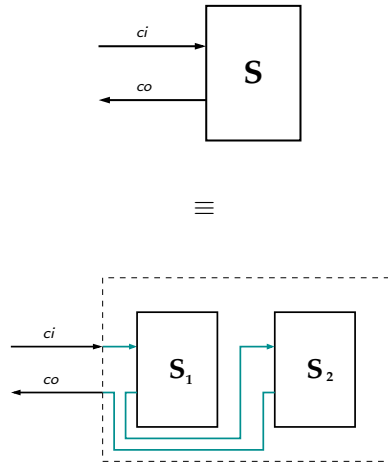
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## Translating $S_1; S_2$



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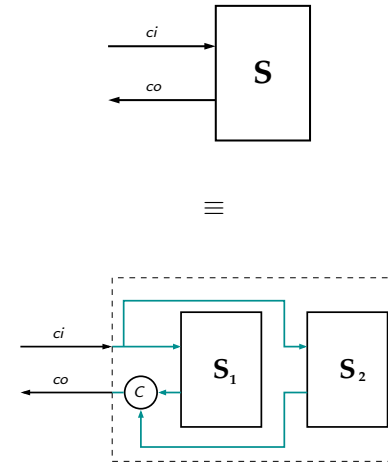
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## Translating $S_1 \parallel S_2$



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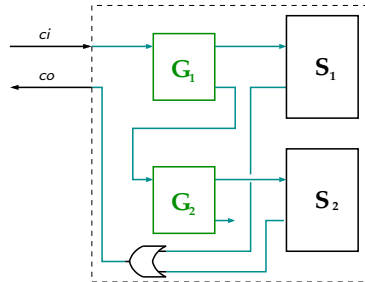
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## Deterministic selection statements



(In this version, only local variables are used)

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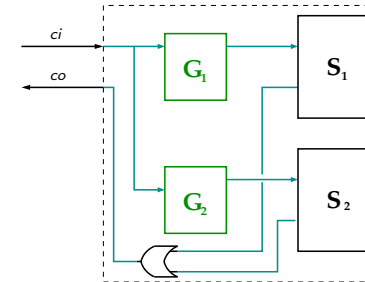
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## Deterministic selection statements



(In this version, only local variables are used)

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