ECE 4250/ENAS 8750
Introduction to VLSI System Design

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What is ECE 4250?

"Computers in the future may weigh no more than 1.5 tons."
— *Popular Mechanics, 1949*

"I think there is a world market for maybe five computers."
— *Thomas Watson, Chairman of IBM, 1943*

"I have traveled the length and breadth of the country and talked with the best people, and I can assure you that data processing is a fad that won't last out the year."
— *editor in charge of Prentice Hall business books, 1957*

... so what happened?

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What is ECE 4250?

The microelectronics revolution!

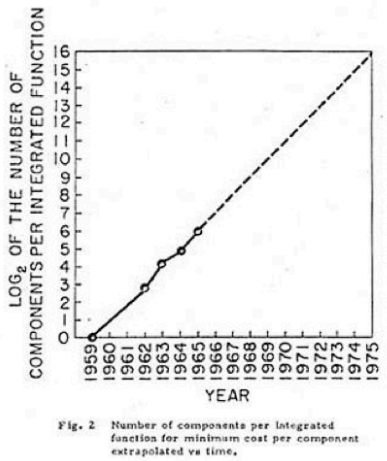

Fig. 2 Number of components per integrated function for minimum cost per component extrapolated vs time.

Moore, 1965

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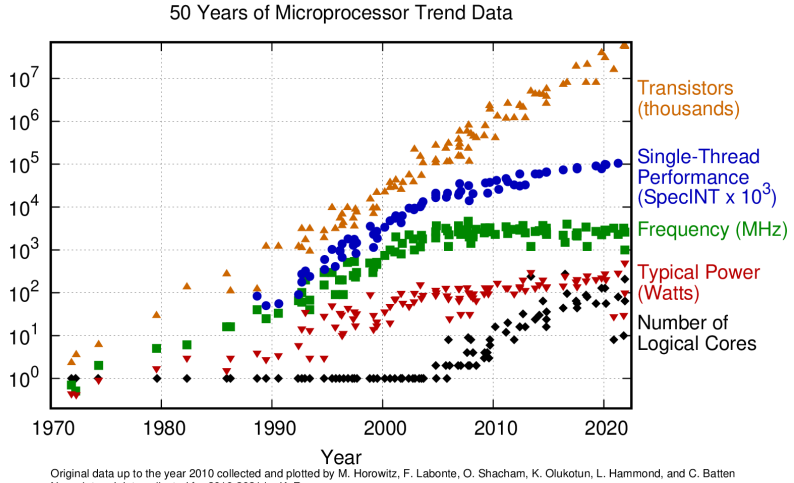
What is ECE 4250?



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Administrivia

- Lectures: 17 HLH 05, MW 11:35-12:50
- WWW: Check announcements regularly!
- Grading:
  - 65% labs (5 labs: 5%+10%+15%+15%+20%)
  - 10% quizzes (9, every week, will drop lowest grade)
  - 20% midterm
  - 5% instructor discretion

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Administrivia

Labs:

- You can do them on your laptop
- Unix environment (Linux): an image will be provided with software pre-installed (additional pieces as needed)
- All tools are written by my research group, or open source

Lab writeup:

- One page executive summary for each lab
- Electronic submission

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Administrivia

Late Policy: 0 (with the usual exceptions)
If you contact me in advance, I can be flexible.

Collaboration:

- Labs are in groups of two or three
- General discussions among students permitted
- Lab work is expected to be done separately

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Administrivia

Text: No required text.

For reference: Weste/Harris, CMOS VLSI Design

Chip:

- "Tape-in" this semester for all students.
- "Tape-out" for students whose designs pass all final checks—hopefully everyone
  - Test chip will arrive in the Spring.

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Projects

Examples from previous years

- Simple microprocessor (default, the last lab)
- Pipelined 8/16-bit RISC processor
- MMX instructions
- FIR filter
- IP packet filter
- Tic tac toe
- Stack machine
- Vector SRAM

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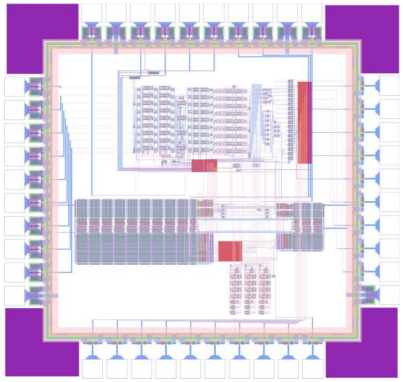
Projects

Tic Tac Toe: 6584 fets



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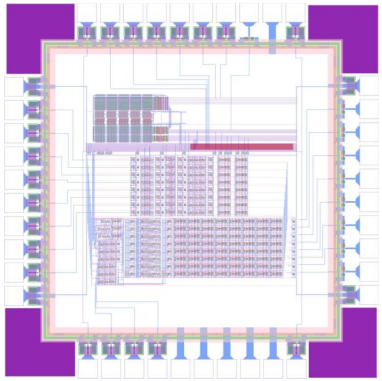
Projects

Stack machine: 5375 fets



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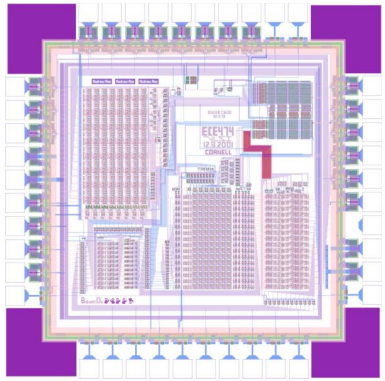
Projects

16-bit RISC processor: 12680 fets



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What is EENG 4250?

Design tools	Design methodology
Optimal use of devices	Managing complexity
Device modeling	Abstraction
Clocked circuits	Clocked + event-driven
Specific implementations	Techniques, tools, and themes in VLSI

Very
Large
Scale
Integration

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Topics

- Introduction
- Transistors
- Switching networks
- Clocking
- Data v/s control
- Datapath circuits
- Memory
- Floorplanning
- Retiming
- Delay optimization
- Power/clock distribution
- Inductance, packaging
- Scaling
- Energy dissipation
- Leakage
- Advanced circuits
- ASIC flow
- Timing
- Multiple clock domains
- Metastability

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Design Flow

- Functional specification
- Architectural specification
- Circuits
- Abstract mask geometry
- Physical masks
- Chip

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The Technology: CMOS

Complementary Metal Oxide Semiconductor

Goals:

- Correctness
- Performance
- Energy efficiency
- ...

"VLSI is a statement about system complexity, not transistor size or circuit performance." – Mead, 1979

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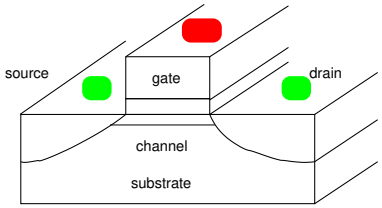
The Device

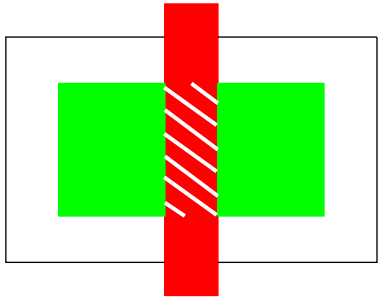
Metal Oxide Semiconductor Field Effect Transistor



Two basic types: *n*-channel and *p*-channel

Geometry

Rotate the device and look from the top:



Abstraction

Mask Geometry

Simplifying assumption:

- all dimensions are multiples of a scaling parameter λ
- *Scalable* CMOS (SCMOS) design rules.

When technology improves, adjust λ and reuse the design!

This abstraction has broken down (more on this later ...)

Ideal scaling

Linear dimension	λ	λ/α
Voltage	V	V/α
Current	I	I/α
Power	VI	VI/α^2
Delay	t	t/α
Energy	VIt	VIt/α^3

... per device.

Ideal scaling

Moore's law: # of transistors doubles every 18 months

Complexity analogy: Seitz and Mead, 1979. Imagine a city where streets are wires with 200m between blocks.

Year	Spacing	Chip size	City
1963	$50\mu m$	$1mm$	town ($4km$)
1975	$10\mu m$	$5mm$	county ($100km$)
1985	$2\mu m$	$10mm$	state ($100km$)
1995	$0.5\mu m$	$20mm$	continent ($8000km$)

Today: $0.003\mu m$ ($3nm$), $28mm$ chip size!

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Ideal scaling

Key observation: abstraction!

Reuse:

- design tools, methods, circuits, abstract geometry

... as long as we understand how scaling works.

Mainstream modern CMOS process:

- Gate: $0.005\mu m$ ($5nm$)
- Voltage: $0.8V$
- FO1 inverter: $< 1ps$ delay

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