EENG 4250/ENAS 8750
Introduction to VLSI System Design

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Datapath: addition and subtraction

Recall: kill-propagate-generate (kpg) codes

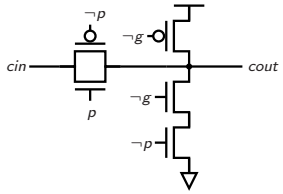
$$\begin{aligned} cout &= (cin \wedge P) \vee G \\ G &= a \wedge b \\ P &= a \vee b \end{aligned}$$

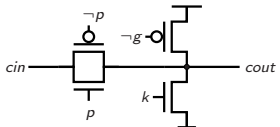
Block codes:

$$G_{01} = G_1 \vee (G_0 \wedge P_1)$$
$$P_{01} = P_0 \wedge P_1$$

Manchester carry chain

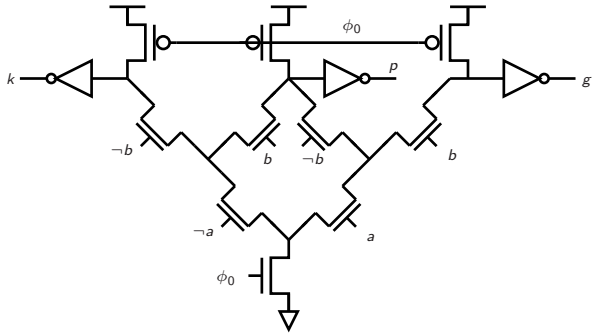
Pass-gate implementation:





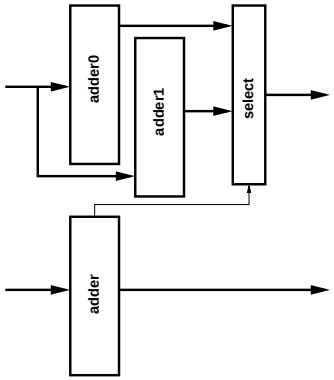
kpg codes

$$\begin{aligned} k &= \neg a \wedge \neg b \\ g &= a \wedge b \\ p &= (a \wedge \neg b) \vee (\neg a \wedge b) \end{aligned}$$



When lookahead is too slow...

Carry select (conditional sum) adder:



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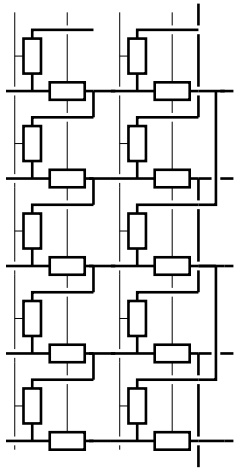
Shifting



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Multiplication

Array multiplier:

- Brute-force solution
- Either add zero, or the operand
- Use lots of full adders

What happens? How fast is this?

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Carry save adders

Trick: you just have to add up bits; the order doesn't matter.

- Full adder takes three bits, produces two

Change the way the carries are connected!
Structure?
Can we do better?

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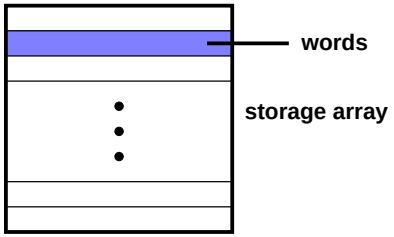
Memories

What makes them different from registers?

- Size
- Speed
- Access patterns

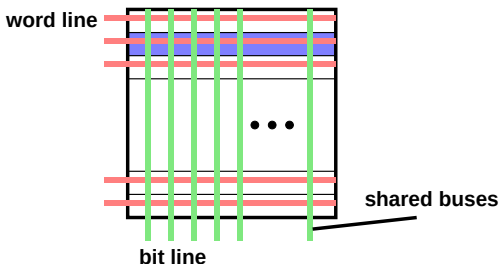
(For small amounts of storage, we use registers.)

Memory organization



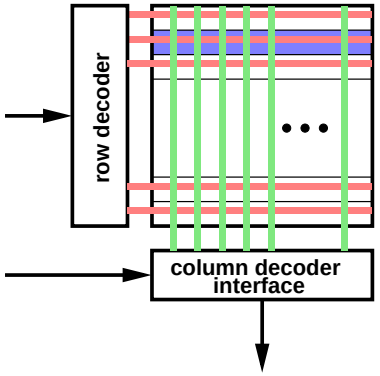
Core: storage elements

Memory organization



Use one set of wires to read the output, another to select the word.

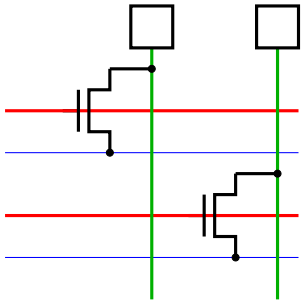
Memory organization



Convert address into selection signals.

Read only memory (ROM)

Read only memory:



Does this look familiar?

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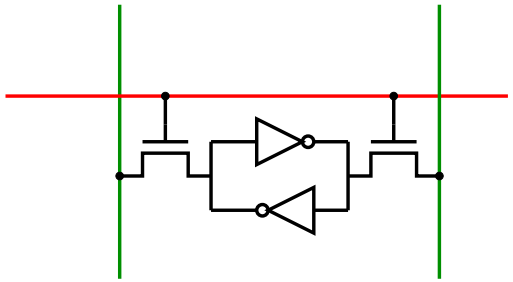
AVLSI

Static RAM

Storage elements are not dynamic.



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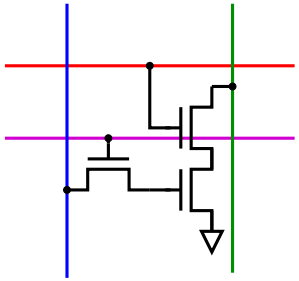
Dynamic RAM

Charge stored on a capacitor.



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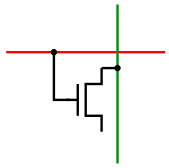
Dynamic RAM

Or even fewer transistors...



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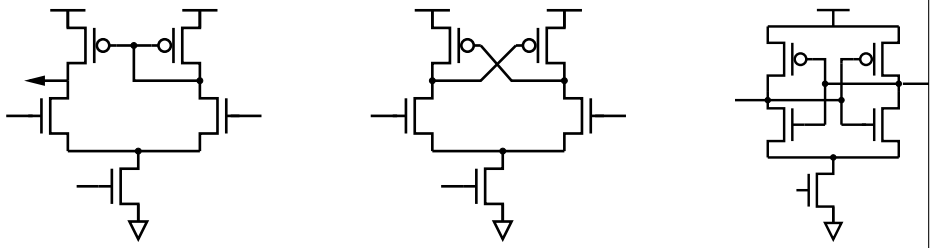
Sense amplifiers



Equalize the bitlines before using the sense amplifier.

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