EENG 4250/ENAS 8750
Introduction to VLSI System Design

Rajit Manohar

Computer Systems Lab

http://csl.yale.edu/~rajit

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Design organization

Logic design:

- Determine necessary functionality
- Identify data dependencies
- Pipelining
- Design datapath and control

Physical design:

- Datapath: simple arrayed cells
- Control: many unique cells
- Run wires straight
- Run data "horizontally," control "vertically"

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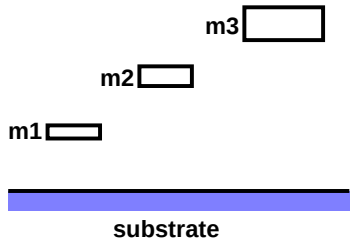

Representative values for sub-micron CMOS technology:

- Metal 1: $R_{\square} = 0.09\Omega/sq$; $C_{sub} = 32aF/\mu m^2$
- Metal 2: $R_{\square} = 0.09\Omega/sq$; $C_{sub} = 16aF/\mu m^2$
- Metal 3: $R_{\square} = 0.05\Omega/sq$; $C_{sub} = 10aF/\mu m^2$

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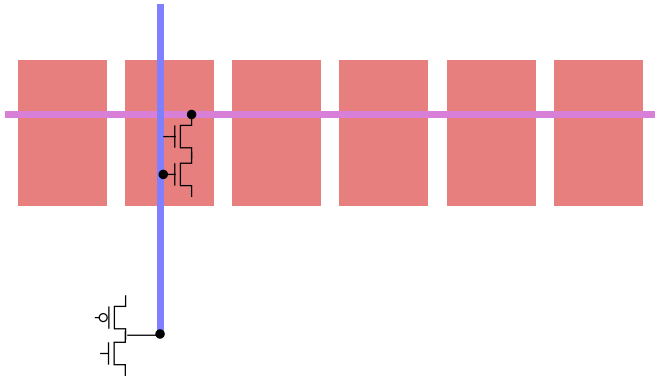

How do we make the buses go faster? The control wires?

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Floorplanning

Top-level layout organization:

- Placement of datapath blocks
- Position of buses and major wiring
- Metal layer usage
- Power, ground, clock distribution

A bad floorplan can be expensive:

- Area
- Cycle time
- Energy

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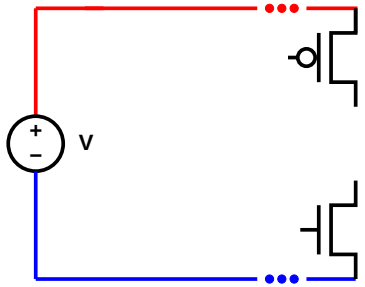
Power and ground

Distributing power/ground should not be an afterthought.



Why might this be a problem? Floorplanning?

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Clock distribution

A serious design challenge...

- *RC* delays don't scale with technology
- Clock *skew*

Tricks:

- Aggressive delay optimization
- Latches are transparent (some skew is ok)
- Multiple phases
- Delay matching
- Dynamic phase adjustment

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Clock Distribution and Inductance

Clock distribution trees:

- Careful layout
- Plan clock distribution wires
- H-trees were popular; *RC*-trees are used

Inductance:

- Long wires
- Bonding wires to the package
- Board traces

Signals? Power supply?

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I/O

To get signals on and off a chip:

- *Pads*: big metal "sandwich"
- Input/output pins on the chip are bonded to pads
- Wires from layout connected to pads
- Pad design rules don't scale
  (bonding machines constrain them)

Organization:

- Periphery of chip
- Multiple layers
- Array pads

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Pads

Multiple types:

- Input pads
- Output pads
- Bidirectional pads
- Tristate pads

Others:

- Power supply pads
- Level shifting pads
- Analog (bare) pads
- LVDS pads, etc etc.

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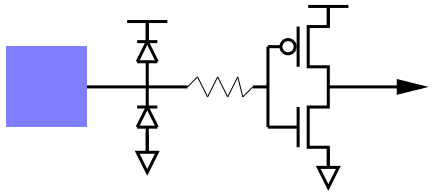
Input pads

What do we know about the inputs from off-chip?



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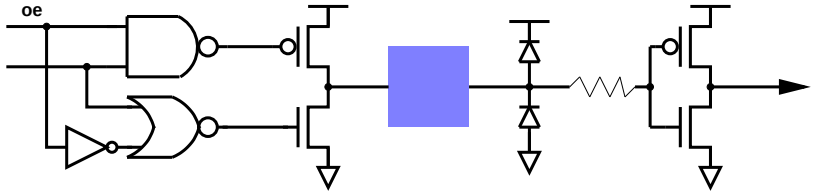
Bidirectional and tristate pads

Why do we use this particular structure?



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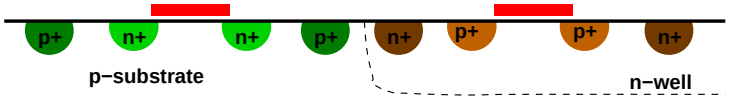
Guard rings

Used to isolate sensitive parts of the circuit from "noisy" parts.



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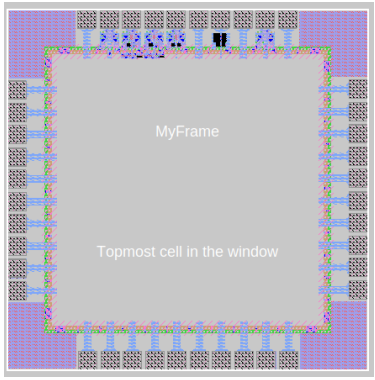
Pad frame



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