EENG 4250/ENAS 8750
Introduction to VLSI System Design

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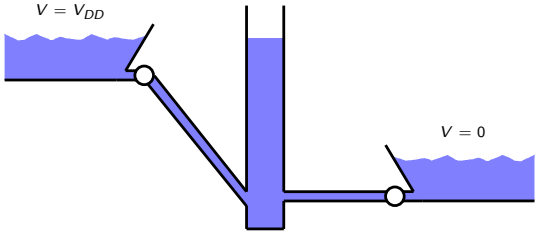
Circuits: a simple analogy

Fluid Model

- Amount of water = charge (coulombs)
- Flow rate = current (amperes = coulombs/sec)
- Height of water = potential (volts)
- Reservoirs = reference potentials



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Capacitors

Tank = capacitor

- Charge $\propto$ Voltage
- $Q = CV$

I = Current = rate of flow of charge = $\frac{dQ}{dT}$

Normally,

$$I = C\,\frac{dV}{dT}$$

Units: Farads (F)

Order of magnitude in 0.18μm CMOS: 0.1$fF/\mu m^2$

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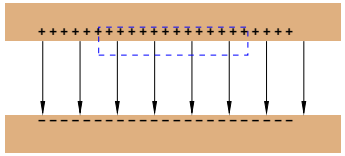
Capacitors



Electrostatics: $\nabla \cdot \mathbb{E} = \frac{\rho}{\epsilon_0}$

$Q = \sigma A$ $\qquad$ $\epsilon_0 = 8.85 \times 10^{-12} F/m$

So: $E = \frac{\sigma}{\epsilon}$ $\qquad$ $\epsilon = k\epsilon_0$

So: $V = \frac{\sigma d}{\epsilon}$

So: $Q = \frac{\epsilon_0 A}{d} V$

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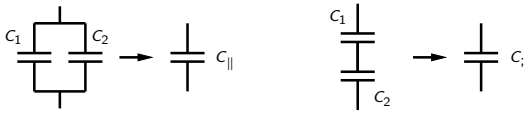
Capacitors

Capacitance $C = \epsilon A/d$

When we draw geometry, we control A

So for us $C = (\epsilon/d)A$



Series/parallel combination of capacitors:

- $C_{\|} = C_1 + C_2$
- $\frac{1}{C_;} = \frac{1}{C_1} + \frac{1}{C_2}$

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Resistors

The diameter of the pipe restricts the flow rate.

- $I = V/R$, or $I = GV$, or $V = IR$

Units: Ohms (Ω)

Order of magnitude in $0.18\mu m$ CMOS: $0.1\Omega/sq$

Resistance $R = \rho\frac{l}{A}$; $A = w \times t$, t: thickness of wire

So for us $R = (\rho/t)\frac{l}{w}$

$\frac{1}{R_{\|}} = \frac{1}{R_1} + \frac{1}{R_2}$ $R_; = R_1 + R_2$

Conductance $G = \frac{1}{R}$ (mhos or siemens)

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Transistors

Before we understand how transistors work we consider two basic *transport phenomenon* for systems of particles:

- Drift
- Diffusion

Drift: what happens when we apply a force

Diffusion: what happens when there is a non-uniform concentration of particles

Warning: What follows is a highly simplified 1D treatment...

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Drift

Particles in random motion, with a net force $\mathbb{F}$.

- Let t_f be the mean time between collisions
- After collision, let particle velocity be v_T on average

$$F = ma \qquad \delta x = \frac{1}{2}at_f^2 = \frac{F}{2m}t_f^2$$

So:

$$v_{drift} = \frac{\delta x}{t_f} = \frac{Ft_f}{2m} = \frac{qEt_f}{2m} = \mu E$$

where $\mu = \frac{qt_f}{2m}$ *mobility*

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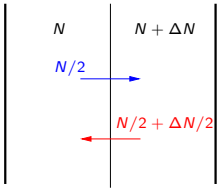
Diffusion



Width of each compartment: $v_T t_f$

Particles that move left: $\Delta N/2 \Rightarrow v_{diff} = -v_T \Delta N/2N$

Finally: $\Delta N \approx \frac{dN}{dx} v_T t_f$

So:

$$v_{diff} = -\frac{1}{2N}\frac{dN}{dx} t_f v_T^2 = -\frac{1}{2N}\frac{dN}{dx} t_f \frac{kT}{m}$$

Diffusion constant: $D = kTt_f/2m = \frac{kT}{q}\mu$

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Boltzmann distribution

When a particle system is in equilibrium, drift and diffusion cancel out.

$$-\frac{1}{2N}\frac{dN}{dx} t_f \frac{kT}{m} = \frac{qEt_f}{2m}$$

i.e.

$$-\frac{1}{N}\frac{kT}{q}\cdot\frac{dN}{dx} = E$$

So:

$$V = -\frac{kT}{q} ln \frac{N}{N_0}$$

Or:

$$N = N_0 e^{-qV/kT}$$

$(U_T = kT/q \approx 25.852mV$ at 300K)

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Transistors

Subthreshold Current

In subthreshold, current is dominated by diffusion.

$$\begin{aligned} I &= \underbrace{WqN}_{charge} v_{diff} = -WqD\frac{dN}{dx} = -WqD\frac{N_D - N_S}{L} \\ &= \frac{W}{L} qDN_0 (e^{-(V_S-\psi_S)/U_T} - e^{-(V_D-\psi_S)/U_T}) \\ &= \frac{W}{L} I_0 e^{\kappa V_G/U_T} (e^{-V_S/U_T} - e^{-V_D/U_T}) \end{aligned}$$

$\psi_S \approx \psi_0 + \kappa V_G$

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Transistors: above threshold

Current is dominated by drift.

$$I = WqNv_{drift} = Q\mu E$$

$\psi_S \approx Q/C = \kappa Q/C_{ox} \Rightarrow E = -\kappa/C_{ox}\frac{dQ}{dx}$

So: $I = -\frac{\mu}{C} Q \frac{dQ}{dx}$

Integrating, we get: $I = \frac{\mu}{2CL}(Q_S^2 - Q_D^2)$

i.e. $I = \frac{W}{L}\frac{\mu C_{ox}}{2\kappa}((\kappa(V_G - V_{T0}) - V_S)^2 - (\kappa(V_G - V_{T0}) - V_D)^2)$

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Simplified

$V_{GS} \leq V_T$ (subthreshold):

$$I_{DS} = \frac{W}{L} I_0 e^{(\kappa V_g - V_s)/U_T} \underbrace{(1 - e^{-V_{DS}/U_T})}_{\approx 1} \approx 0$$

$0 < V_{DS} < V_{GS} - V_T$ (linear):

$$I_{DS} = \mu C_{ox} \frac{W}{L} [(V_{GS} - V_T) V_{DS} - V_{DS}^2/2]$$

$0 < V_{GS} - V_T < V_{DS}$ (saturation):

$$I_{DS} = \mu C_{ox} \frac{W}{L} \frac{(V_{GS} - V_T)^2}{2}$$

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Digital abstraction

We will simplify all this to:

- If the voltage $V(g) > \min(V(s), V(d)) + v_{tn}$, then current flows between s and d until $V(s) = V(d)$ or $V(g) \leq \min(V(s), V(d)) + v_{tn}$.
- If the voltage $V(g) < \max(V(s), V(d)) + v_{tp}$, then current flows between s and d until $V(s) = V(d)$ or $V(g) \geq \max(V(s), V(d)) + v_{tp}$.

Note: $v_{tp} < 0, v_{tn} > 0$ for standard MOSFETs.

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Digital abstraction

Drawing transistors:

nFET: if $V(g)$ is "high" long enough, then $V(s) = V(d)$

pFET: if $V(g)$ is "low" long enough, then $V(s) = V(d)$

Not quite true... let's look at this more closely

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Digital abstraction

Using an nFET:

Remember: current flows when

$$V(g) > \min(V(s), V(d)) + v_{tn}$$

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Digital abstraction

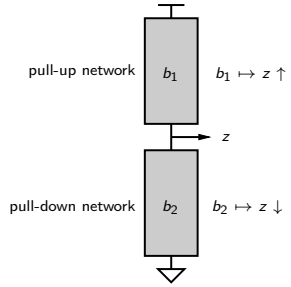
Using a pFET:

Remember: current flows when

$$V(g) < \max(V(s), V(d)) + v_{tp}$$

Switching networks

In general, we have something like:



We only use pFETs in the pull-up and nFETs in the pull-down. What if b_1 and b_2 are false?

Inverting logic

CMOS is said to be "inverting."

Given a one-stage circuit $\mathcal{C}$ computing

$$y = \mathcal{C}(\mathbf{x})$$

where $\mathbf{x}$ is a Boolean vector of inputs, we know that if any component of $\mathbf{x}$ changes from *false* to *true*, the output changes from *true* to *false* or remains unchanged.

Why?