EENG 4250/ENAS 8750
Introduction to VLSI System Design

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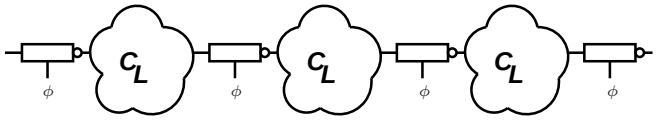
Yale

AVLSI

Single phase clocking

Simple pipeline:



Clock input:

Timing constraints for correctness? (race-through)

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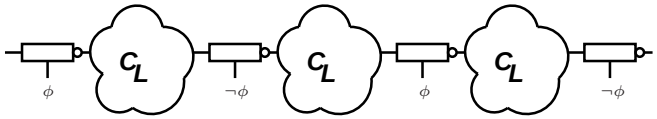
AVLSI

Single phase clocking

Better pipeline structure:



Clock input:

Timing constraints for correctness?

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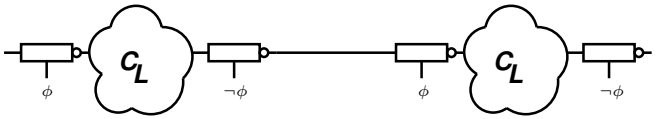
AVLSI

Single phase clocking

Special case:



Clock input:

Timing constraints for correctness?

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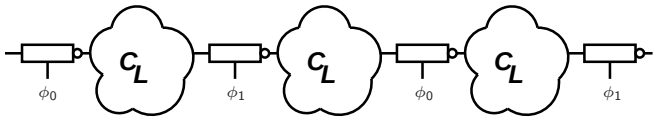
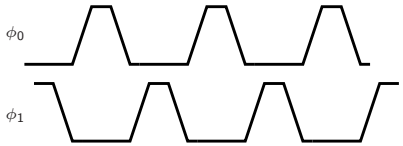
Two phase non-overlapping clocks

Safe pipeline structure:



Clock input:



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AVLSI