EENG 4250/ENAS 8750
Introduction to VLSI System Design

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AVLSI

Faster logic

We'd like to compute with nfets;

In particular, lots of parallel nfets...

Restoring combinational logic: results in long series pfet chains.

How do we fix this?

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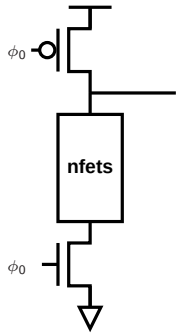
Precharge logic

Idea: each section of combinational logic has active and idle periods.



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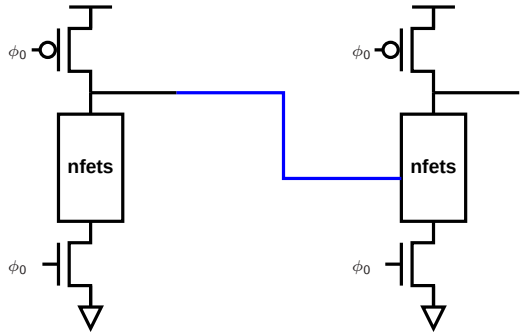
Precharge logic

How do we cascade these stages?



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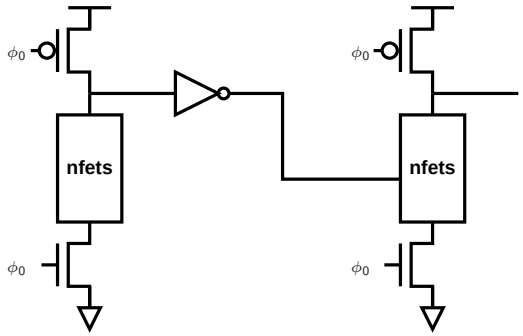
Domino logic

Or like this?



... how do we generate the complement of a signal?
... and what does the pipeline look like?

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Charge sharing

We can mitigate charge-sharing problems in domino stages.

- Identify nodes in the nfet network that might cause problems
- Precharge those nodes to *Vdd* too!

If we keep the clocked gate at the "foot" of the domino stage, this is safe. (Why?)

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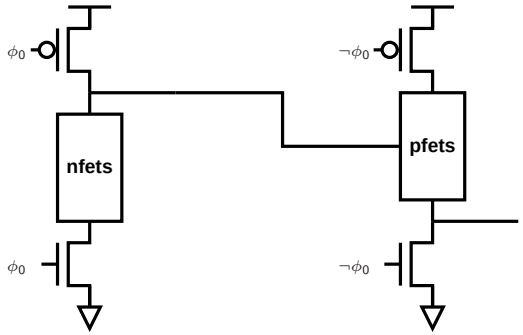
np Domino logic

Alternating nfet and pfet stages:



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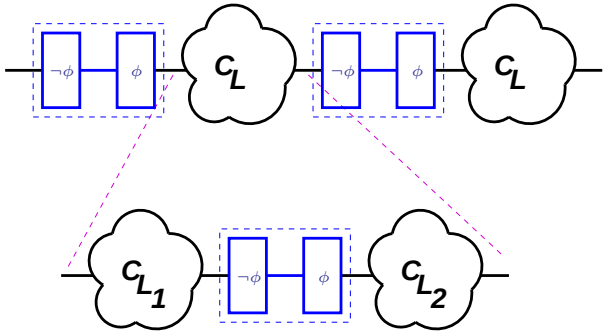
Retiming

Problem: can't meet timing budget.



Obvious "solution:" add a pipeline stage...

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