# EENG 4250/ENAS 8750
# Introduction to VLSI System Design

**Rajit Manohar**

Computer Systems Lab

http://csl.yale.edu/~rajit

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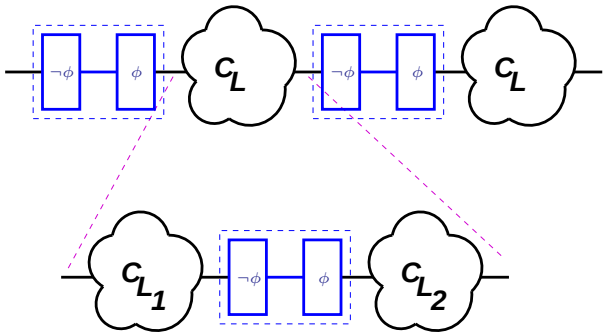
## Retiming

Problem: can't meet timing budget.




Obvious "solution:" add a pipeline stage...

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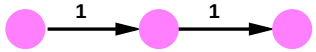
## Retiming

Graph formulation:

- nodes correspond to "clouds" of combinational logic
- directed edges have integer weights
  - weight = # of flops on the edge
  - direction = direction of information flow

Simple pipeline:

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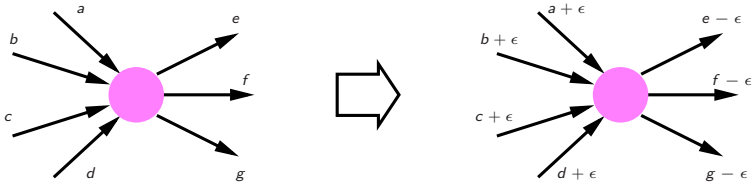
## Retiming

One safe transformation:




For a node $n$, we can define $\delta(n)$ to be this $\epsilon$.

What does this correspond to, and why is it safe?

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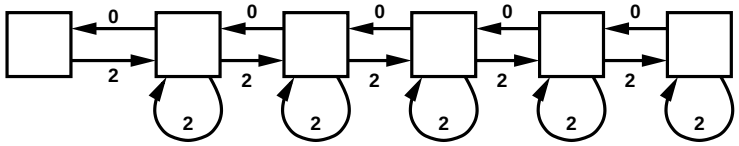
## Retiming

Broadcasting information:




When can we retime the graph to make sure all edges have $> 0$ flops?

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## Retiming

Start with a network with weights that are either zero or positive.

Theorem: Given a network with weighted graph $G$, there exists a suitable function $\delta$ on the nodes of $G$ if and only if $G - 1$ has no negative weight cycles.

Proof?

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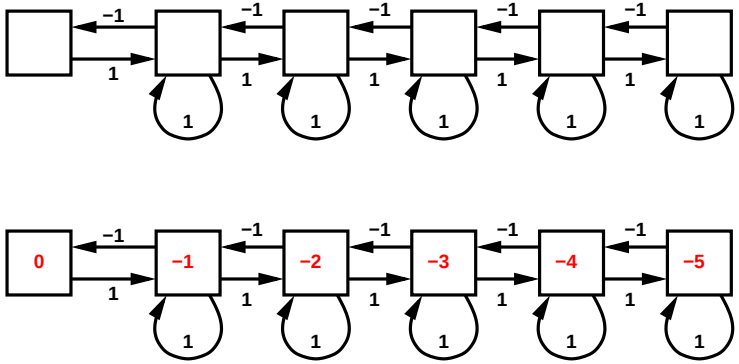
## Retiming

Broadcast problem:

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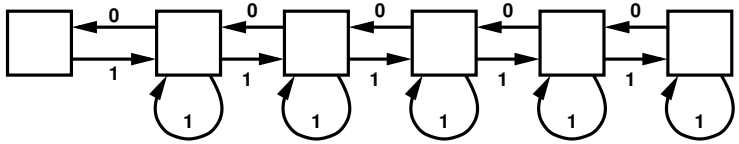
## C-slow retiming

What about:




One approach: scale register count by a factor $c$ (e.g. $c = 2$)

- Called $c$-slow retiming

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