A High-Performance Asynchronous FPGA: Test Results

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Abstract

We report test results from a prototype asynchronous FPGA (AFPGA) implemented in TSMC's 0.18μm CMOS process. The AFPGA uses SRAM-based configuration bits with pipelined logic blocks and switch boxes. Test results demonstrate a throughput of 674 MHz at 1.8 V.

1. Introduction

Asynchronous FPGA designs were proposed as a way to combat the problems of clock distribution in FPGAs, as well as to exploit the data-dependent nature of circuit delays by not having to time the circuit using the worst-case delay path [1]. Initial asynchronous FPGA designs borrowed heavily from clocked FPGAs, and attempted to map a netlist of asynchronous logic gates to a configurable netlist of a fixed set of gates. However, technology mapping an asynchronous logic gate is complicated by the fact that an asynchronous control signal must have no switching hazard.

We have developed an asynchronous FPGA (AFPGA) architecture that operates on different principles [5, 6]. Instead of a gate-level mapping, we map the *functionality* of the asynchronous logic to the FPGA directly. Our AFPGA corresponds to an array of one-bit configurable clockless pipeline stages, with a pipelined interconnect providing high-throughput operation for long routes.

We completed the VLSI design of a test chip with a small array of AFPGA cells. The test chip was fabricated in TSMC's $0.18\mu m$ CMOS process available through the MOSIS VLSI service. We report the results of our measurements in this paper. At room temperature and with a supply voltage of 1.8 V, we measured a throughput of 674 MHz. To our knowledge, the only other published configurable asynchronous circuit that was fabricated was the PCA-1 architecture, and they reported a peak throughput of 20 MHz in a $0.35\mu m$ CMOS process [2]. Even adjusting for feature size, our results are better by over an order of magnitude.

2. AFPGA Design and Test Chip

The AFPGA is an island-style FPGA architecture, and is loosely based on the Xilinx Virtex FPGA [7]. Each logic block contains a 4-input lookup table (LUT), an internal state unit, a conditional unit, and various buffers and copies required to implement asynchronous logic. Switch boxes are pipelined as well, which implies that system throughput does not degrade when long routes are used. A detailed description of the AFPGA can be found in [6].

We used the `magic` VLSI layout editor [3] for the design of the test chip, with MOSIS deep-submicron scalable design rules. Our prototype contains a 5×5 array of logic blocks, where the arrayable tile is $2017\lambda \times 1017\lambda$, where $\lambda = 0.09\mu m$. Replicating this tile at the specified pitch in each dimension results in an AFPGA array in which reset, power, ground, and signal wires are correctly connected. This area includes five horizontal and five vertical routing tracks. The VLSI layout for the AFPGA array is shown in Figure 1. While the fabrication technology supports six metal layers, we did not use the sixth layer for the AFPGA cell or routing. Our current implementation only has nearest-neighbor routing; future implementations of larger arrays will use the additional metal layer for a segmented routing architecture and additional routing tracks.

To measure the throughput of the AFPGA, an on-chip

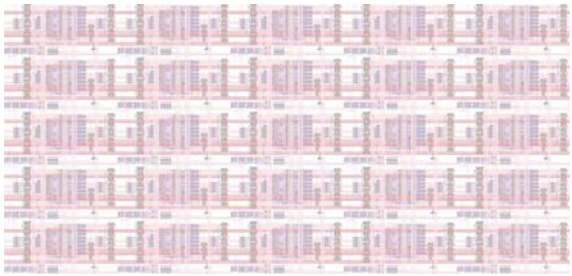

Figure 1. VLSI layout of a 5×5 AFPGA array

asynchronous counter was used. The counter is triggered whenever a fixed AFPGA cell receives a data input, and an I/O pad is connected to a signal in the high-order counter bit-cell as a way to implement a simple frequency divider; this permits a low-frequency off-chip measurement.

3. Test Results

The peak AFPGA throughput is limited by the 4-LUT. For the measurements, the throughput of the AFPGA was determined by configuring the logic block to use the 4-LUT. Other parts of the AFPGA operate at higher frequencies, but we do not expect them to be representative of the achievable AFPGA throughput. Details on variation of throughput with configuration can be found in [4].

The TSMC $0.18\mu m$ run for our test chip had threshold voltages of 0.52 V and -0.54 V at room temperature for short-channel n-channel and p-channel devices respectively. At nominal temperature without any external cooling (294K), the AFPGA was found to be functional without interruption of operation when the supply voltage was varied from 130 mV to 2.3 V. (We did not attempt to exceed 2.3 V for any of our measurements.) The measured throughput varied from 1.7 KHz at 130 mV to 870 MHz at 2.3 V. The throughput at 1.8 V was found to be 674 MHz, close to the estimated 700 MHz from HSPICE simulation [6].

We also made high-temperature and low-temperature measurements using a cryostat. Since we had to thread long wires through the cryostat to make our measurements and due to space constraints in the test cavity, all our measurements correspond to the average frequency at a specific voltage in the presence of large power supply noise (160 mV peak-to-peak at 1.8 V).

At an environmental temperature of 400 K, the AFPGA operated correctlyfrom 340 mV to 2.3 V. The throughput at 340 mV was found to be 1.47 MHz, while the throughput at 2.3 V was 625 MHz. The throughput at 1.8 V was found to be 490 MHz. At 77 K (liquid N_2) environmental temperature, the AFPGA operated correctly from 810 mV to 2.3 V. The throughput at 810 mV was 31 MHz, and it was 1.12 GHz at 2.3 V. At 1.8 V, the throughput was 857 MHz.

A complete voltage sweep at various temperatures is shown in Figure 2. The temperature dependence of the threshold voltage is clearly indicated by the "kink" in the throughput measurements. Note that the AFPGA continues to operate sub-threshold, because our asynchronous design style does not make any major timing assumptions. The chip operated correctly while we continuously varied the voltage and temperature; we did not have to re-initialize the circuit for each data point in Figure 2. For reference, we also show the frequency of operation reported by Xilinx for their Virtex FPGA series scaled to compensate for the change in feature size from $0.22\mu m$ to $0.18\mu m$ [7].

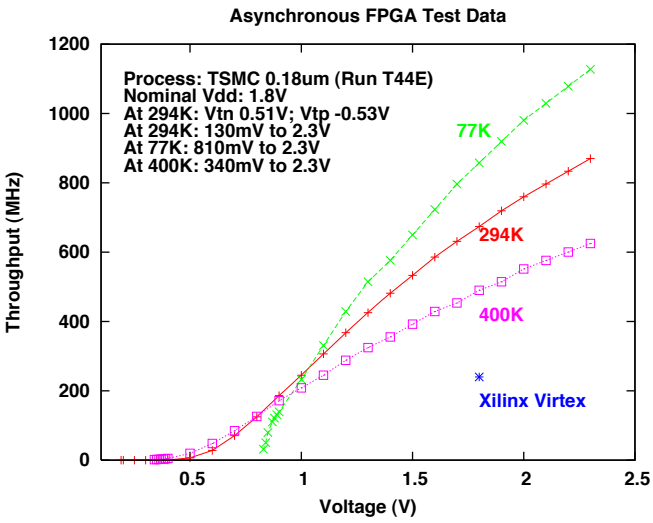

Figure 2. AFPGA throughput measurements

4. Conclusions

We have reported test measurements from a high-performance asynchronous FPGA. The results demonstrate correct and robust operation over a wide range of voltages and temperatures, and compare favorably to the baseline clocked FPGA on with the AFPGA design was based.

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References

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